INTERNATIONAL TELECOMMUNICATION UNION

ITU-T G.975.1

TELECOMMUNICATION
STANDARDIZATION SECTOR
OF ITU

(02/2004)

SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

Digital sections and digital line system – Optical fibre submarine cable systems

Forward error correction for high bit rate DWDM submarine systems

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ITU-T Recommendation G.975.1

FORWARD ERROR CORRECTION FOR HIGH BIT RATE DWDM SUBMARINE SYSTEMS

(Geneva, 2004)

Summary

This Recommendation describes the Forward Error Correction (FEC) functions that have higher-correction ability than RS (255,239) code defined in G.975 for the high bit rate DWDM submarine cable systems. In appendix, super FEC schemes, which have higher-correction ability than RS (255,239) code, are also described. The use of this super FEC function in submarine terminal transmission equipments (TTEs) should not be considered as mandatory.

1. Scope

This Recommendation describes the Forward Error Correction (FEC) functions that have higher-correction ability than RS (255,239) code defined in G.975 in the optical fibre submarine cable systems. This Recommendation also describes the system requirement concerning supervision for the submarine cable systems. The applications being addressed in this Recommendation are both optically amplified repeatered systems (Recommendation G.977) and repeaterless optical systems (Recommendation G.973). The use of this FEC function in submarine terminal transmission equipments (TTEs) should not be considered as mandatory.

It is not the intention of this Recommendation to pursue the transverse compatibility of the system. Therefore the selection of the FEC frame structures described in this Recommendation is a matter of joint engineering.

The transmission signal under consideration could be STM-16, STM-64, STM-256, ODU-1, ODU-2, and ODU-3, because submarine system could be considered as one of the IaDI applications defined in G.872. This doesn't mean that the bit rate is restricted within above-mentioned signals.

2. References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published.

ITU-T Recommendation G.691 (2003), *Optical interfaces for single-channel STM-64, STM-256 and other SDH systems with optical amplifiers*

ITU-T Recommendation G.693 (2003), *Optical interfaces for intra-office systems*

ITU-T Recommendation G.707 (2000), *Network node interface for the synchronous digital hierarchy (SDH).*

ITU-T Recommendation G.709 (2003), *Interfaces for optical transport network (OTN).*

ITU-T Recommendation G.798 (2002), *Characteristics of Optical Transport Networks (OTN) Hierarchy Equipment Functional Blocks.*

ITU-T Recommendation G.805 (2000), *Generic Functional Architecture of Transport Networks.*

ITU-T Recommendation G.872 (2001), *Architecture of Optical Transport Networks.*

ITU-T Recommendation G.957 (1999), *Optical interfaces for equipments and systems relating to the synchronous digital hierarchy*

ITU-T Recommendation G.959.1 (2003), *Optical Transport Network Physical Layer Interfaces.*

ITU-T Recommendation G.972 (2000), *Definition of terms relevant to optical fibre submarine cable systems.*

ITU-T Recommendation G.973 (2003), *Characteristics of repeaterless optical fibre submarine cable systems.*

ITU-T Recommendation G.975 (2000), *Forward error correction for submarine systems*

ITU-T Recommendation G.977 (2003), *Characteristics of optically amplified optical submarine cable systems*

IEEE Std 802.3 (2002), *Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications*

3. Terms and Definitions

3.1 Terms defined in other Recommendations

This ITU-T Recommendation uses the following terms defined in other Recommendations:

Synchronous Digital Hierarchy (SDH): See ITU-T G.707.

Synchronous Transport Module (STM): See ITU-T G.707.

Optical fibre submarine cable system: See ITU-T G.972.

Terminal Transmission Equipment (TTE): See ITU-T G.972.

Optical power budget: See ITU-T G.972.

Service channel: See ITU-T G.972

Order wire channel: See ITU-T G.972

Line error ratio: See ITU-T G.972

Forward Error Correction (FEC): See ITU-T G.972

FEC frame: See ITU-T G.972

FEC encoder: See ITU-T G.972

FEC decoder: See ITU-T G.972

Block code: See ITU-T G.975

Cyclic code: See ITU-T G.975

Systematic code: See ITU-T G.975

Information word: See ITU-T G.975

Codeword: See ITU-T G.975

3.2 Definitions

For the purpose of this Recommendation, the following definitions apply.

3.2.1. **Coding Gain:** Coding gain means the improvement of received optical sensitivity by FEC, without considering penalty by bit rate increasing.

3.2.2. **Net Coding Gain:** Net coding gain means the improvement of received optical sensitivity by FEC, with considering penalty by bit rate increasing.

4. Abbreviations

This Recommendation uses the following abbreviations:

BER	Bit Error Ratio
EDFA	Erbium-Doped Fibre Amplifier
FEC	Forward Error Correction
GF	Galois Field
RS	Reed-Solomon
BCH	Bose-Chaudhuri-Hocquenghem
TTE	Terminal Transmission Equipment
TTI	Trail Trace Identifier
DWDM	Dense Wavelength Division Multiplexing
NCG	Net Coding Gain

5. Super FEC features

5.1 General principles of super FEC function

In order to increase transmission bit rate, distance, and capacity utilized in the DWDM technology, the super FEC, which has more effective error correction than RS (255, 239) code, could be required for the submarine optical fibre systems.

Figure 1 outlines the fact that the encoding and decoding procedures are performed at the Terminal Transmission Equipment (TTE) level only, on electrical signals, and benefit the overall optical fibre submarine cable system, which comprises the optical fibre and possibly optical modules such as optical amplifiers using EDFA technology.

The super FEC function essentially comprises:

- a super FEC encoder in the transmit Terminal Transmission Equipment (TTE) that accepts information bits and adds computed redundant symbols, producing encoded data at a higher bit rate;
- a super FEC decoder in the receive Terminal Transmission Equipment (TTE) that performs the error correction while extracting the redundancy to regenerate the data that was encoded by the FEC encoder.

The transmission signal under consideration could be STM-16, STM-64, STM-256, ODU-1, ODU-2, and ODU-3. GbE and/or 10GbE may be required for interface of submarine TTEs. However, this doesn't mean that the bit rate is restricted within above-mentioned signals.

Several super FEC schemes, their features and correction ability are described in Appendix I.

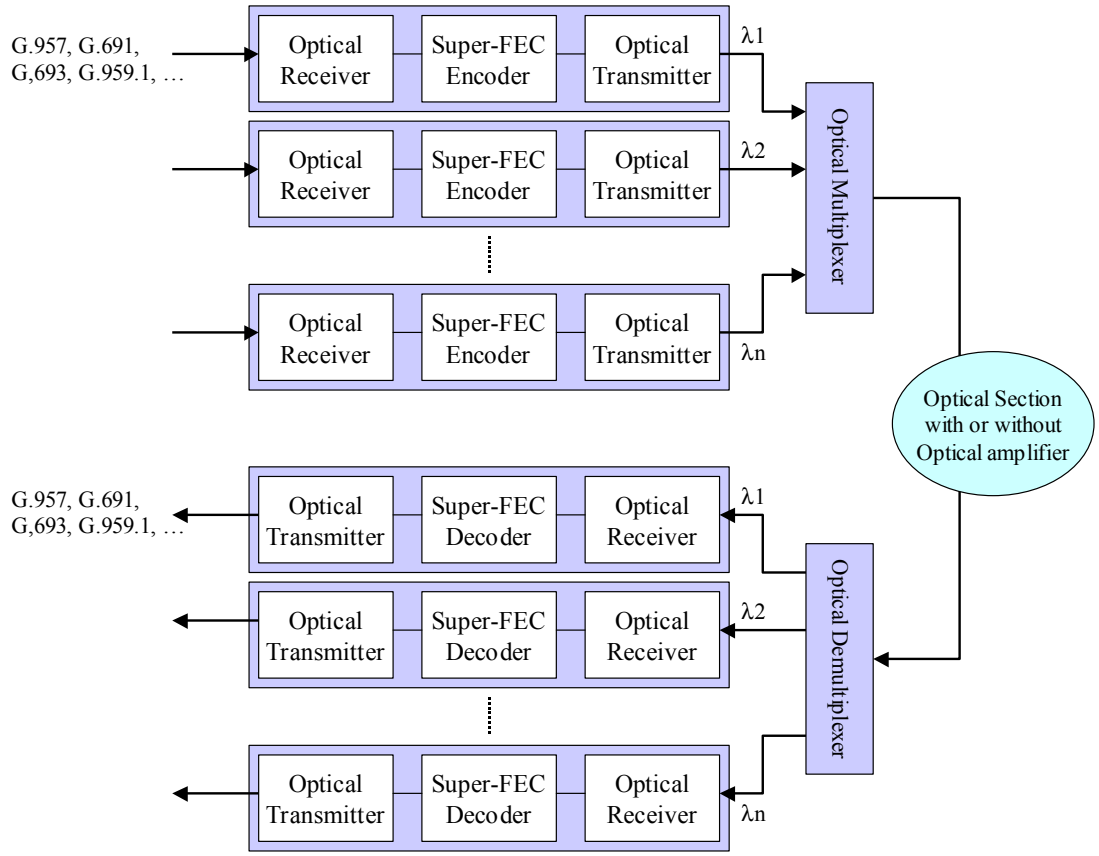

Figure 1/G.975.1 – Block diagram of DWDM submarine optical fibre system

5.2 Super FEC scheme

A Forward Error Correction (FEC) scheme is commonly utilized for both submarine and terrestrial optical fibre systems, which are defined in G.975 and G.709, respectively. In those Recommendations, Reed-Solomon (255,239) code is defined as FEC scheme.

In order to achieve higher correction ability, several super FEC schemes are considered. For example, super FEC that uses a combination of two FEC codes, is well known, such as [RS code + RS code], [BCH code + BCH code], [RS code + BCH code], and etc.

For other technique, super FEC scheme that uses longer word length is also well known.

6. Definition of super FEC function

6.1 Definition

Super FEC code: Various super FEC codes are considered. RS (255,239) that is defined in G.975 and G.709 has 5.6dB Net Coding Gain at 10^{-12} decoder output BER. This recommendation defines the super FEC code that has higher correction ability than RS (255,239). Improvement value for super FEC compared with RS (255,239) is for further study.

Outer code / Inner code: Figure 2 shows Outer could and Inner code for super FEC scheme utilizing two concatenated FEC codes.

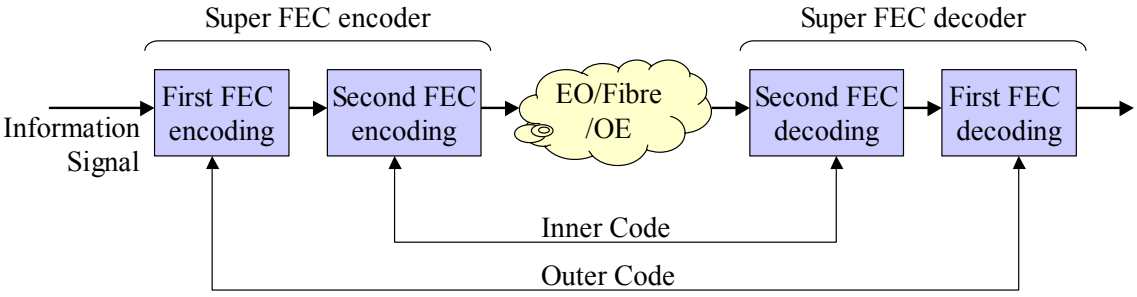

Figure 2/G.975.1 Outer Code and Inner Code

Hard decision decoding: Hard decision decoding refers to the use of a single quantization level in bit sampling, resulting in binary bit information provided to the decoding process.

Soft decision decoding: For the same received waveform, soft decision decoders make use of multiple levels of quantization (typically three or more).

6.2 Super FEC code algorithm

A super FEC algorithm depends on target features, such as correction ability, latency, and/or etc. Detailed algorithms for super FEC code are described in Appendix I.

6.3 Properties for super FEC code

Super FEC properties depend on its FEC scheme. One super FEC scheme may take pride in higher correction ability, other super FEC scheme may show lower latency. Detailed properties for super FEC code are described in Appendix I.

6.4 Super FEC frame structure

Frame structures are described in Appendix I.

7. Parameters for super FEC

The super FEC code is defined in several aspects, such as the feasibility of circuit operation speed, requirement from system transaction delay and theoretical optimum redundancy ratio. Each

condition is described in the following sub-section. The parameters described in this section are represented in Appendix I.

7.1 Correction ability

Error correction ability is indicated by various parameters, such as BER characteristics, net-coding gain and etc. Though all parameters are closely related, each indication is useful for the estimation of super FEC code. The following parameters should be described for each super FEC code in Appendix I.

7.1.1. BER characteristics

A BER characteristic for FEC is shown as relation between BER of decoder input signal and BER of corrected output signal. And this BER improvement by FEC is the most interested characteristics and indicates FEC correction ability.

7.1.2. Coding Gain

In the case of randomly distributed errors within the encoded line signal, a FEC decoder reduces the line or raw BERin (B_{in}) to a required reference BER (B_{ref}) value within the payload signal. Coding gain could therefore be regarded as the relation of these Bit Error Ratios. In order to define a coding gain parameter as a more system related parameter, the BER reduction by the FEC is usually transformed into a dB value based on a theoretical reference system. It is common practice to define the coding gain as the reduction of signal-to-noise ratio at a reference BER.

$$Coding\_Gain = 20\log_{10}\left[erfc^{-1}\left(2\,B_{ref}\right)\right] - 20\log_{10}\left[erfc^{-1}\left(2\,B_{in}\right)\right] \quad \text{(dB)}$$

7.1.3. Net Coding Gain

NCG is characterized by both the code rate R (R<1, the code rate R is the ratio of bit rate without FEC to bit rate with FEC) and the maximum allowable BERin (B_{in}) of the input signal of the FEC decoder, which can be reduced to a reference BERout=B_{ref} by applying the FEC algorithm. Furthermore, NCG should refer to a binary symmetric channel with added white Gaussian noise:

$$Net\_Coding\_Gain = 20\log_{10}\left[erfc^{-1}\left(2\,B_{ref}\right)\right] - 20\log_{10}\left[erfc^{-1}\left(2\,B_{in}\right)\right] + 10\log_{10} R \quad \text{(dB)}$$

with $erfc^{-1}$ the inverse of the complementary error function, erfc(x) = 1- erf(x)

7.1.4. Q limit

Q limit means the minimum required allowable Q factor of the input signal for the receiver decision circuit in order to achieve a reference BER ($B_{ref} \approx$ BERout). The Q factor is the signal-to-noise ratio at the decision circuit in voltage or current units, and is typically expressed by:

$$Q = \frac{\mu_1 - \mu_0}{\sigma_1 + \sigma_0}$$

$\mu_{1/0}$: The mean value of the marks/spaces voltages or currents

$\sigma_{1/0}$: The standard deviations of the marks/spaces voltages or currents

The mathematical relations to BER (in case of non-FEC operation) when the threshold is set to the optimum value are

$$BER = \frac{1}{2} erfc(\frac{Q}{\sqrt{2}})$$

Table 1 is summary table format for correction ability of a super FEC scheme of above parameters. In order to clarify correction ability, all value should be put into table. Summary table for correction ability are described in Appendix I.

Table 1/G.975.1 - Summary table format for correction ability

Input BER	Output BER	Net coding gain (dB)	Coding gain (dB)	Q limit (dB)
	10^{-9}			
	10^{-10}			
	10^{-11}			
	10^{-12}			
	10^{-13}			
	10^{-14}			
	10^{-15}			

7.2 Redundancy ratio

Redundancy ratio depends on the super-FEC methods. It describes the ratio between the number of information bits covered by the FEC and the number of bits after encoding comprising the same information plus the added redundancy information. It does not take into account any management overhead or stuffing, like as described by G.709.

Some methods have the same redundancy ratio as G.709 or G.975, even though the correction ability is better than those.

7.3 Latency

FEC transaction may introduce transmission delay for FEC encoding, decoding, interleaving and de-interleaving. This delay may be described as a physical time value for a given transmission rate. Alternatively, it may be given as the number of intermediately stored information bits while in the process of encoding/decoding. In most cases this second number is independent of the actual transmission rate.

8. Supervision

When definition of super FEC frames, OH (Over Head) functions shall be described to achieve some maintenance function. These functions that are described in this section are used for measure the transmission performance. But concrete way is for further study.

8.1 Signal quality supervision

To evaluate the transmission condition, some error counting technique is required, such as BIP error counting or counting for the number of FEC error correction bit. Performance monitoring using error counting is mandatory for this Recommendation.

8.2 Connectivity supervision

To prevent miss-connection, trail trace such as TTI is needed

Appendix I

Super FEC schemes

I.1 Overview

Table I. 1 shows an over view of super FEC schemes that are described in this Appendix I. Each super FEC scheme is described following sub-clause that is represented in Table I. 1.

Table I. 1/G.975.1 - Overview of super FEC schemes

Sub-Clause	FEC scheme	
	Concatenated or Non-concatenated	**Used FEC code**
I.2	Concatenated FEC	Outer code: RS (255, 239) Inner code: CSOC (n_0/k_0=7/6, J=8)
I.3	Concatenated FEC	Outer code: BCH (3860, 3824) Inner code: BCH (2040, 1930)
I.4	Concatenated FEC	Outer code: RS (1023, 1007) Inner code: BCH (2047, 1952)
I.5	Concatenated FEC (Soft Decision capable)	Outer code: RS (1901, 1855) Inner code: Extended Hamming Product Code (512, 502) x (510, 500)
I.6	Non-concatenated FEC	LDPC Code
I.7	Concatenated FEC	Two orthogonally concatenated BCH codes
I.8	Non-concatenated FEC	RS (2720, 2550)
I.9	Concatenated FEC	Two interleaved extended BCH (1020, 988) codes

I.2 RS (255, 239) / CSOC (n_0/k_0=7/6, J=8) super FEC code

I.2.1 Overview

This sub-clause describes a super-FEC scheme, which provides higher error correction capability than RS (255,239) code. Figure I. 1 shows the super-FEC scheme. The super-FEC scheme uses concatenated RS and convolutional self-orthogonal code (CSOC). RS (255,239) is used as the outer

code. CSOC (n_0/k_0=7/6, J=8) is used as the inner code, where k_0 is the number of bits to be encoded, n_0 is the number of coded bits and J is the number of orthogonal check sets. The interleaver and deinterleaver are used between the inner and outer code.

Concatenated codes can apply iterative decoding. Also, CSOCs can apply iterative decoding independently. These techniques can improve the error correction capability without increasing the coding rate. The number of iteration is vendor specific.

The super-FEC scheme provides 7.95 dB net coding gain at 1E-12 corrected BER with 24.48% redundancy, by using three times iterative CSOC decoding.

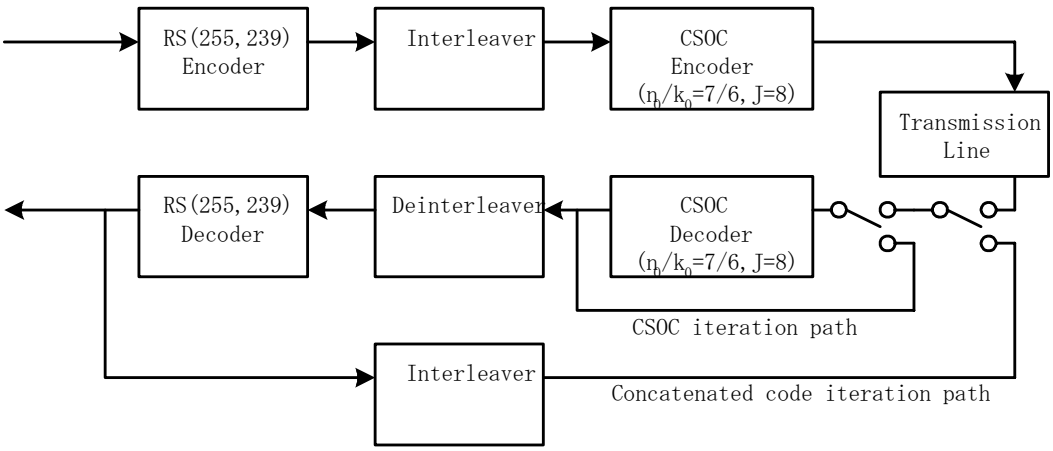

Figure I. 1/G.975.1 - Super-FEC scheme

I.2.2 FEC algorithm

The super-FEC scheme uses concatenated RS (255,239) and CSOC (n_0/k_0=7/6, J=8). The detail specification of RS (255,239), CSOC (n_0/k_0=7/6, J=8) and frame structure are described in I.2.2.3.

I.2.2.1 RS (255,239) code

The RS (255,239) code is a non-binary code (the FEC algorithm operates on 8-bit symbols) and belongs to the family of systematic linear cyclic block codes.

The generator polynomial of the code is given by:

$$G(D)=\prod_{i=0}^{15}\left(D-\alpha^{i}\right) \quad \text{(I.1)}$$

where α is a root of the binary primitive polynomial $x^8 + x^4 + x^3 + x^2 + 1$. A data byte ($d_7$, d_6, ..., d_1, d_0) is identified with the element $d_7 \cdot \alpha^7 + d_6 \cdot \alpha^6 + \ldots + d_1 \cdot \alpha^1 + d_0$ in GF (256), the finite field with 256 elements. The RS (255,239) codeword consists of 239 information bytes and 16 parity bytes. The RS (255,239) can correct up to 8 symbol errors in a single codeword.

I.2.2.2 CSOC (n_0/k_0=7/6, J=8) code

CSOCs are defined by their generator polynomials. The super-FEC code applies following generator polynomials.

$$
\begin{aligned}
G^{(5)}(D) &= 1 + D^{35} + D^{80} + D^{119} + D^{161} + D^{193} + D^{209} + D^{269} \\
G^{(4)}(D) &= 1 + D^{87} + D^{173} + D^{192} + D^{197} + D^{217} + D^{251} + D^{258} \\
G^{(3)}(D) &= 1 + D^{31} + D^{82} + D^{93} + D^{94} + D^{96} + D^{200} + D^{218} \\
G^{(2)}(D) &= 1 + D^{91} + D^{99} + D^{114} + D^{120} + D^{166} + D^{170} + D^{297} \\
G^{(1)}(D) &= 1 + D^{13} + D^{22} + D^{49} + D^{77} + D^{348} + D^{385} + D^{418} \\
G^{(0)}(D) &= 1 + D^{69} + D^{95} + D^{112} + D^{142} + D^{152} + D^{210} + D^{263}
\end{aligned}
\qquad \text{(I.2)}
$$

Fig.I1-2 shows CSOC (n_0/k_0=7/6, J=8) encoding and decoding scheme. The CSOC encoder appends a parity bit to each group of six information bits, and transmits seven coded bits in sequence. The parity sequence P (D) is expressed as

$$P(D) = \sum_{i=0}^{5} M^{(i)}(D) G^{(i)}(D) \quad \text{(I.3)}$$

where $M^{(i)}(D)$ is the information sequence.

The CSOC decoder generates parity checksum sequence S (D) using an encoder replica. Parity checksum sequence S (D) is calculated as

$$
\begin{aligned}
S(D) &= [P(D) + F(D)] + \sum_{i=0}^{5} [M^{(i)}(D) + E^{(i)}(D)] G^{(i)}(D) \\
&= [\sum_{i=0}^{5} M^{(i)}(D) G^{(i)}(D) + F(D)] + \sum_{i=0}^{5} [M^{(i)}(D) + E^{(i)}(D)] G^{(i)}(D) \qquad \text{(I.4)} \\
&= \sum_{i=0}^{5} E^{(i)}(D) G^{(i)}(D) + F(D)
\end{aligned}
$$

where $E^{(i)}(D)$ is the error sequence on the information sequence $M^{(i)}(D)$. F(D) is the error sequence on the parity sequence.

CSOC (n_0/k_0=7/6, J=8) supplies six sets of eight orthogonal parity checksums. A set is used to check one information bit. The information bit is estimated to be error by threshold decoder if the number of parity checksum equal to one in the set is threshold value (Th) and over. Threshold value should be more than J/2. CSOCs can applies iterative decoding by using independently.

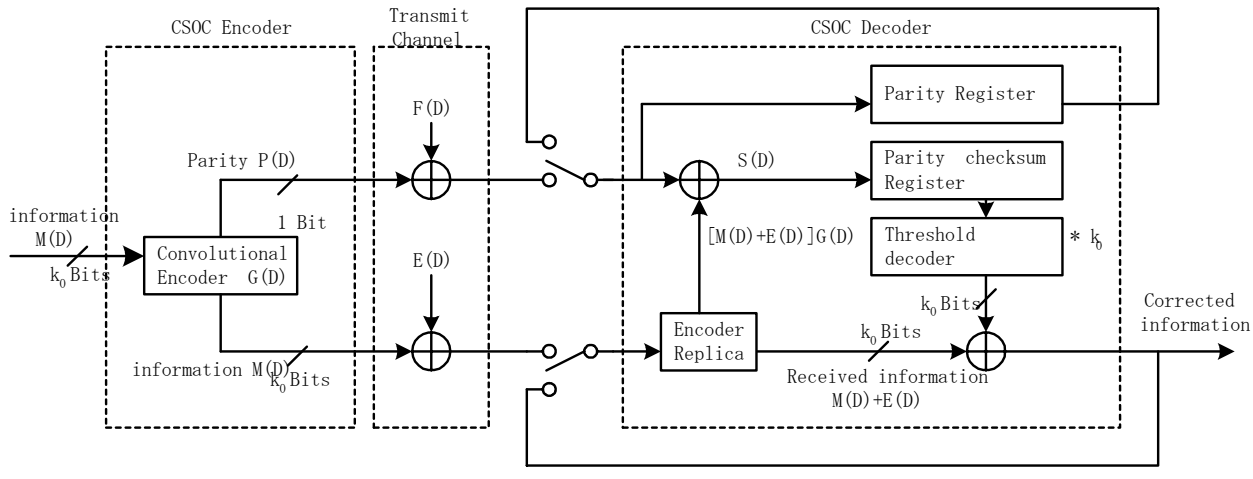

Figure I. 2/G.975.1 - CSOCs encoder and decoder

I.2.2.3 Frame structure

Figure I. 3 shows frame format fed from RS encoder to interleaver. This frame format is named "RS frame format" for convenience sake. RS frame format consists of 16 RS (255,239) codewords.

Figure I. 4shows frame format fed from interleaver to CSOC encoder. This frame format is named "interleaved RS frame format".

Figure I. 5 shows frame format fed from CSOC encoder to transmission line. This frame format is named "CSOC frame format". $m^{(i)}_j$ means j degree coefficient of information sequence polynomial $M^{(i)}(D)$. p_j means j degree coefficient of parity sequence polynomial P(D). Note that CSOC encoders don't process termination at frame boundary.

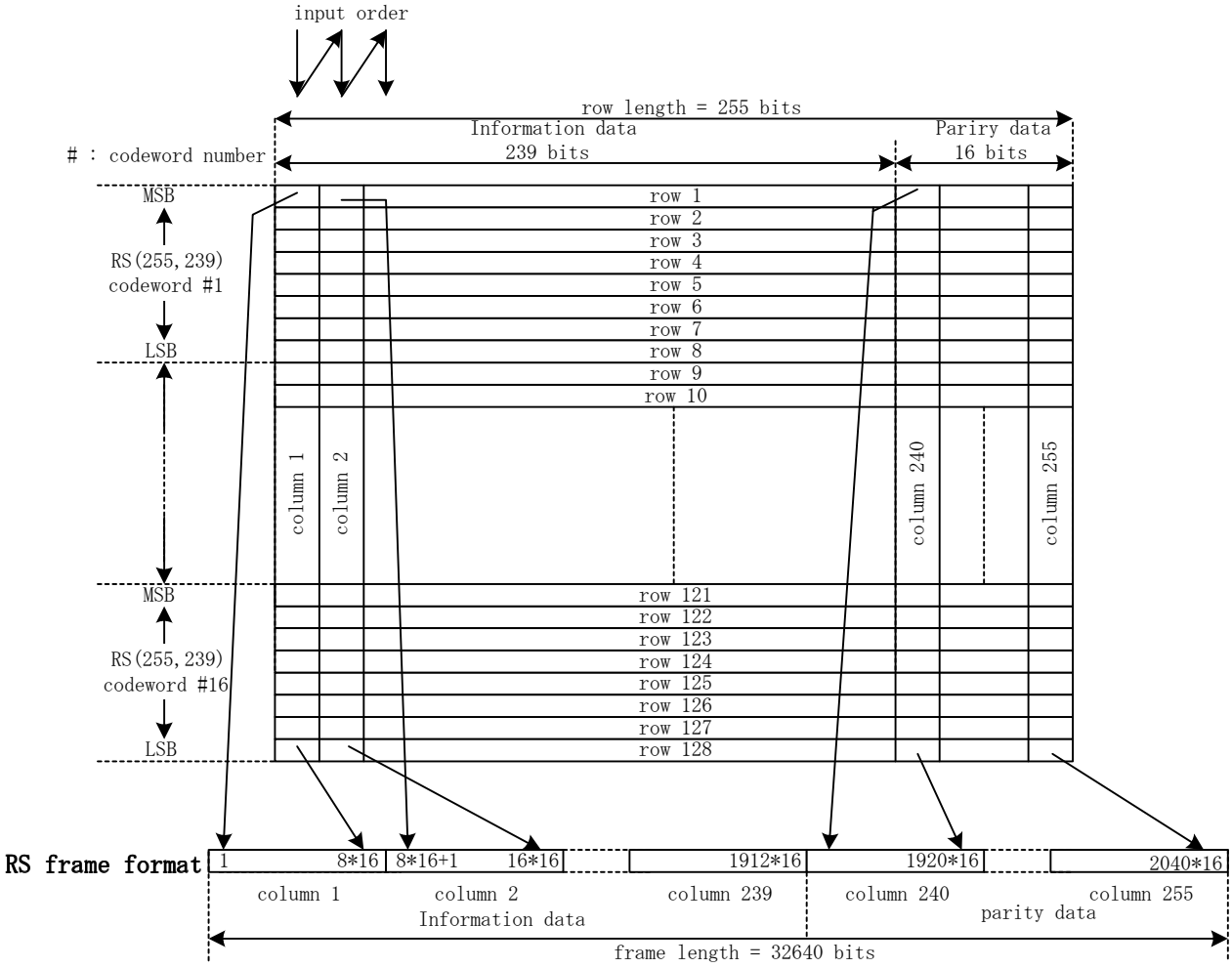

Figure I. 3/G.975.1 - RS frame format

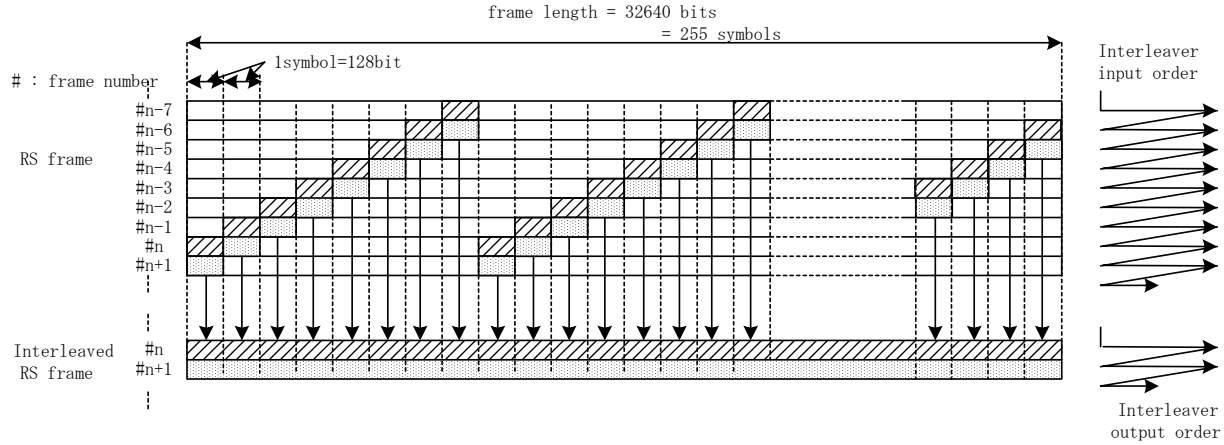

Figure I. 4/G.975.1 - Interleaved RS frame format

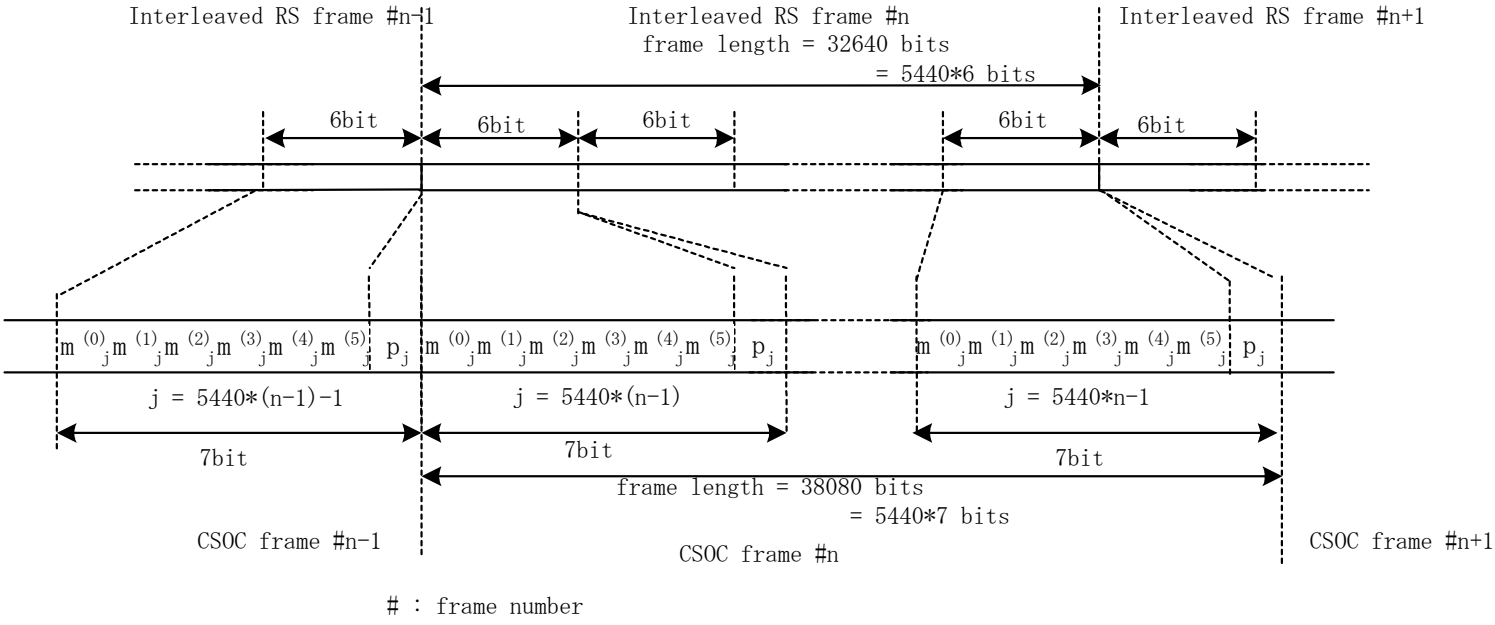

Figure I. 5/G.975.1 - CSOC frame format

I.2.3 Error correction ability

Error correction ability of the super-FEC code depends on the number of iteration times and threshold values of CSOC decoder. Figure I. 6 shows an example of the super-FEC decoder. This decoder iterates CSOC decoding three times. The threshold value of the first, second and third CSOC decoder is seven, six and five respectively. Table I.2 and Figure I.7 show-summary of error correction ability. Figure I.7 shows a comparison of error correction ability between RS (255, 239) and super-FEC decoder.

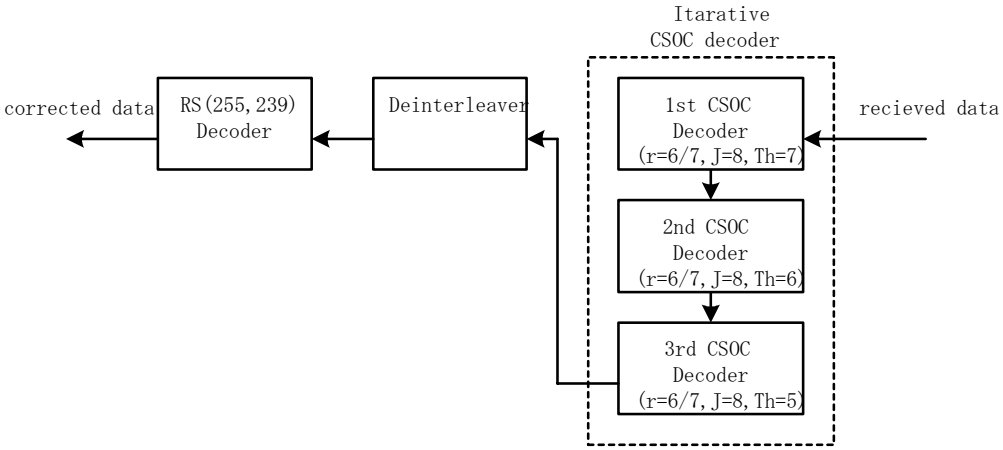

Figure I. 6/G.975.1 - An example of the super-FEC decoder

Table I. 2/G.975.1 – Summary for correction ability

Input BER	Output BER	Net coding gain (dB)	Coding gain (dB)	Q-limit (dB)
6.50E-03	1.00E-09	6.70	7.66	7.9022
6.30E-03	1.00E-10	7.19	8.13	7.9410
6.05E-03	1.00E-11	7.59	8.54	7.9908
5.80E-03	1.00E-12	7.95	8.90	8.0421
5.60E-03	1.00E-13	8.29	9.24	8.0843
5.40E-03	1.00E-14	8.60	9.55	8.1278
5.20E-03	1.00E-15	8.88	9.83	8.1724
5.00E-03	1.00E-16	9.12	10.07	8.2183

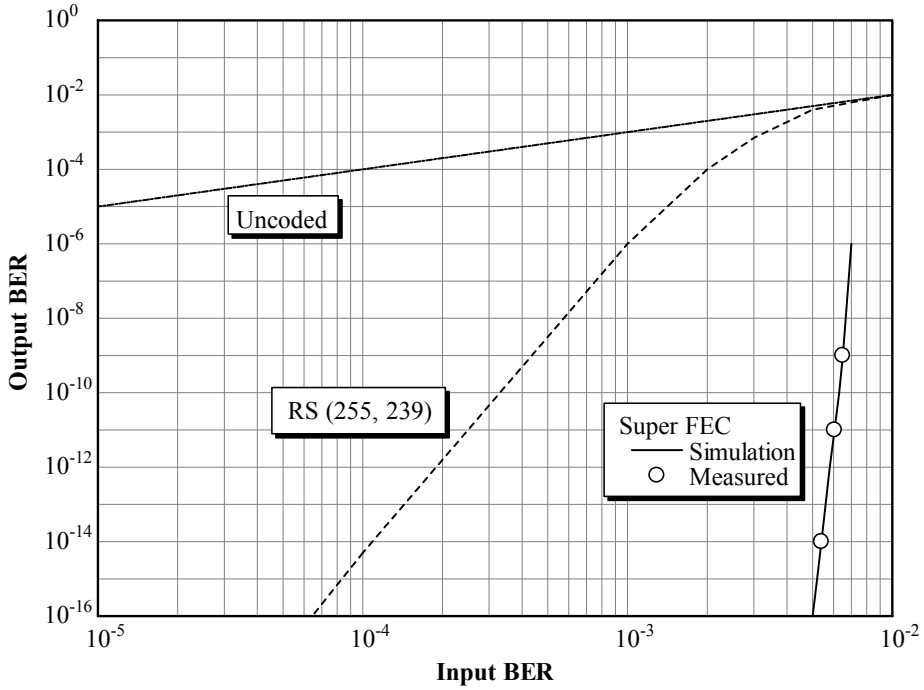

Figure I. 7/G.975.1 – BER characteristics of the super-FEC decoder

I.2.4 Redundancy ratio

Redundancy ratio of the super-FEC code is 24.48%.

I.2.5 Latency

The super-FEC code has an around 25(μs) delay for 10Gbit/s payload throughput, typically.

I.2.6 Property

The super-FEC code has an advantage of low complexity. It is well known that CSOC has an advantage of simple implementation.

I.3 Concatenated BCH super FEC codes

I.3.1 Overview

This sub-clause describes a super-FEC scheme, which provides higher error correction capability than RS (255,239) code. Figure I. 8 shows the super-FEC scheme. The super-FEC scheme uses concatenated BCH codes. BCH (3860, 3824) is used as the outer code. BCH (2040, 1930) is used as the inner code. The interleaver and deinterleaver are used between the inner and outer code.

Concatenated codes can apply iterative decoding. This technique can improve the error correction capability without increasing the coding rate. The number of iteration is vendor specific.

The super-FEC scheme provides 7.98 dB net coding gain at 1E-12 corrected BER with 6.69% redundancy, by using three times iterative decoding.

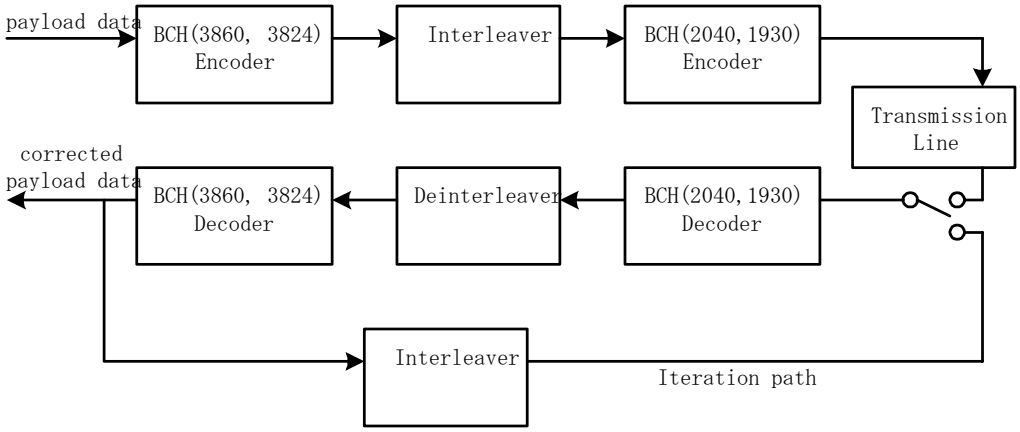

Figure I. 8/G.975.1 - Super-FEC scheme

I.3.2 FEC algorithm

The super-FEC scheme uses concatenated BCH (3860, 3824) and BCH (2040, 1930). The detail specification of BCH (3860, 3824), BCH (2040, 1930) and frame structure are described in I.3.2.3

I.3.2.1 BCH (3860, 3824) code

The BCH (3860, 3824) code is a binary code. The generator polynomial of the code is given by

$$G(x)=M_1(x)M_3(x)M_5(x)$$

$$M_i(x)=\prod_{j=1}^{12}\left(x-\alpha^{i*j}\right)$$

where $M_i(x)$ are minimal polynomials and α is a root of the binary primitive polynomial $x^{12}+x^{11}+x^8+x^6+1$. The BCH (3860, 3824) codeword consists of 3824 information bits and 36 parity bits. The BCH (3860, 3824) can correct up to 3 bit errors in a single codeword.

I.3.2.2 BCH (2040, 1930) code

The BCH (2040, 1930) code is a binary code. The generator polynomial of the code is given by

$$G(x)=M_1(x)M_3(x)M_5(x)M_7(x)M_9(x)M_{11}(x)M_{13}(x)M_{15}(x)M_{17}(x)M_{19}(x)$$

$$M_i(x)=\prod_{j=1}^{11}\left(x-\alpha^{i*j}\right)$$

where $M_i(x)$ are minimal polynomials and α is a root of the binary primitive polynomial $x^{11}+x^2+1$. The BCH (2040, 1930) codeword consists of 1930 information bits and 110 parity bits. The BCH (2040, 1930) can correct up to 10 bit errors in a single codeword.

I.3.2.3 Frame structure

Figure I. 9 shows frame format fed from BCH (3860, 3824) encoder to interleaver. This frame format is named “BCH (3860, 3824) frame format” for convenience sake. BCH (3860, 3824) frame format consists of eight BCH (3860, 3824) codewords. One BCH (3860, 3824) codeword consists of 3824 information bits and 36 parity bits.

Figure I. 10 shows frame format fed from interleaver to BCH (2040, 1930) encoder. This frame format is named “interleaved BCH (3860, 3824) frame format”.

Figure I. 11 shows frame format fed from BCH (2040, 1930) encoder to transmission line. BCH (2040, 1930) encoder replaces dummy data of BCH (3860, 3824) frame to parity check data. BCH (2040, 1930) frame format consists of 16 BCH (2040, 1930) codewords. One BCH (2040, 1930) codeword consists of 1930 information bits and 110 parity bits. The information bits consist of 1912 payload bits and 18 parity bits of BCH (3860, 3824).

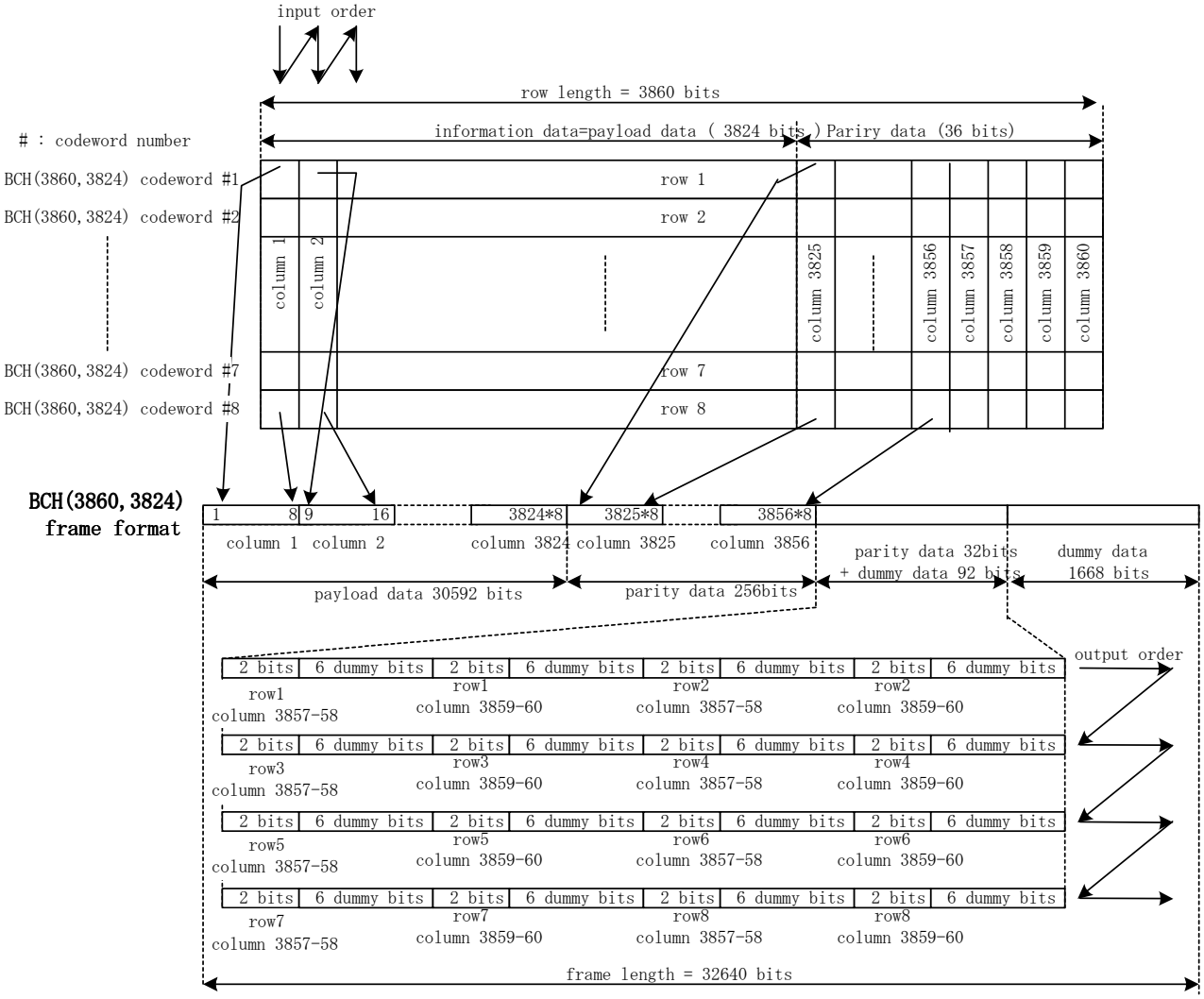

Figure I. 9/G.975.1 - BCH (3860, 3824) frame format

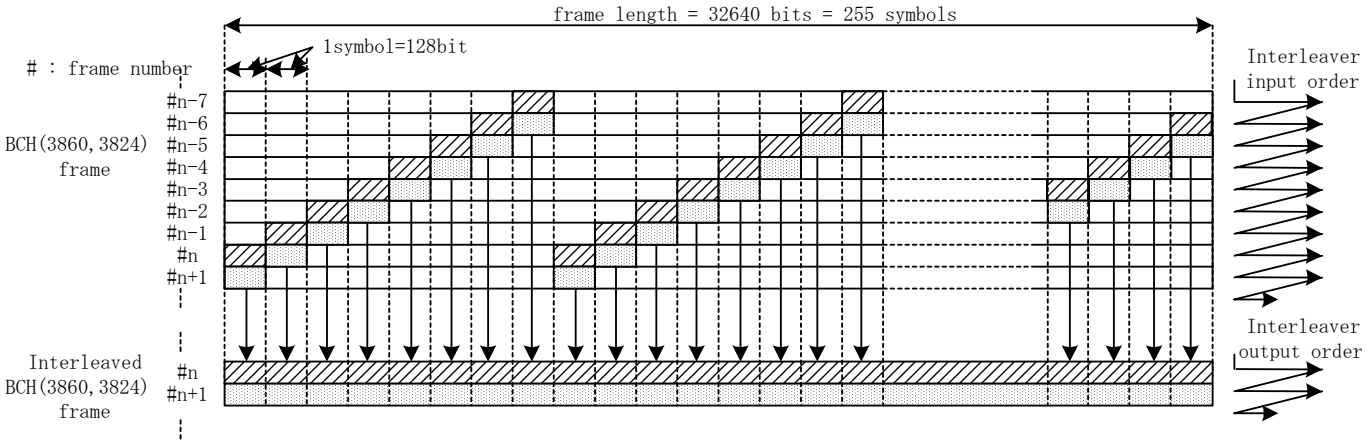

Figure I. 10/G.975.1 - Interleaved BCH (3860, 3824) frame format

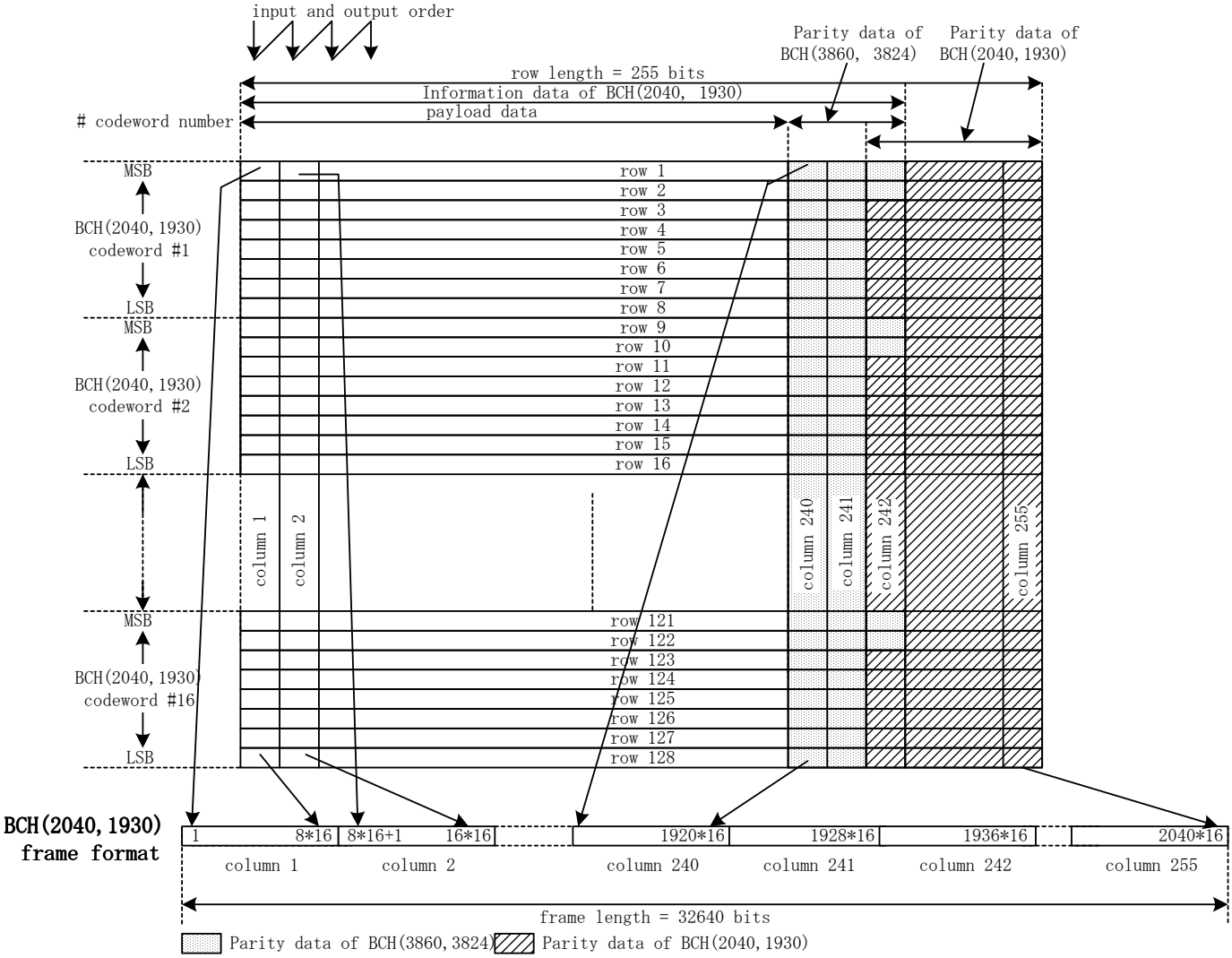

Figure I. 11/G.975.1 - BCH (2040, 1930) frame format

I.3.3 Error correction ability

Error correction ability of the super-FEC code depends on the number of iteration times. Table I.3 and Figure I. 12 show error correction ability when using three times iterative decoding.

Table I. 3/G.975.1 - Summary for correction ability

Input BER	Output BER	Net coding gain (dB)	Coding gain (dB)	Q-limit (dB)
3.50E-03	1.00E-09	6.66	6.94	8.6171
3.44E-03	1.00E-10	7.15	7.44	8.6356
3.37E-03	1.00E-11	7.59	7.87	8.6575
3.30E-03	1.00E-12	7.98	8.26	8.6798
3.25E-03	1.00E-13	8.35	8.63	8.6959
3.20E-03	1.00E-14	8.68	8.96	8.7123
3.15E-03	1.00E-15	8.99	9.27	8.7288
3.10E-03	1.00E-16	9.26	9.54	8.7455

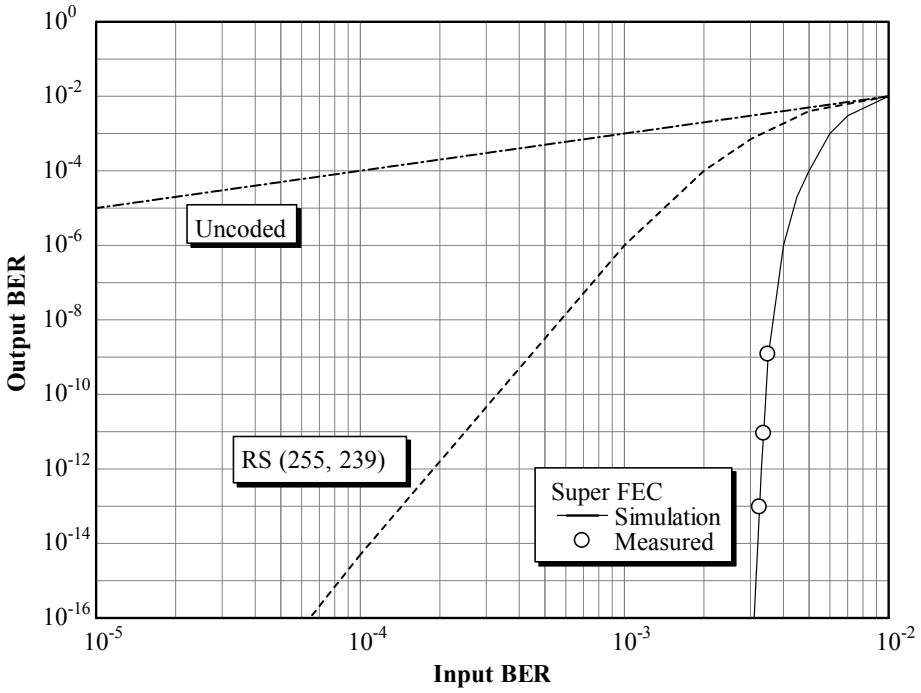

Figure I. 12/G.975.1 – BER characteristics of the super-FEC decoder

I.3.4 Redundancy ratio

Redundancy ratio of the super-FEC code is 6.69%.

I.3.5 Latency

The super-FEC code has an around 100(μs) delay for 10Gbit/s payload throughput, typically.

I.3.6 Property

The super-FEC scheme is rate adapted to G.709 and G.975 frame. There is no additional overhead compared to G.709 and G.975 frame with RS (255,239) encoding.

I.4 RS(1023,1007)/BCH (2047,1952) Super FEC Code

I.4.1 Overview

This Super FEC consists of 2 interleaved codes:

RS(1023,1007) parent outer code, m=10 T=8

BCH (2047,1952) parent inner code, m=11 T=8

These 2 interleaved codes are targeted at providing additional coding gain on the standard G.709 ODU payload while maintaining the exact data rates at the G.709 OTU, i.e. 7% overhead.

I.4.2 Supe FEC Algorithm

I.4.2.1 Code Interleaving

The ODU payload consists of 16x239x4x8 bits = 122368 bits in total. These 122368 bits are divided into 16 groups and are then encoded with 15 RS(781,765) and 1 RS(778,762) code, both of which are shortened codes of the parent code listed above. Note that the parent code above operates on an m=10 Galois Field, so data is grouped into dectets and are operated on accordingly. If we number the ODU payload bits as odu[0], odu[1] up to odu[122367], then the interleaving can be clearly explained. Keep in mind that odu[0] is the first transmitted bit, followed by odu[1] and so on up to odu[122367]. i.e. in G.709 terms, {odu[0], odu[1], odu[2], odu[3], odu[4], odu[5], odu[6], odu[7]} = 0xf6, the first OA1 byte in the G.709 frame.

Using this convention, we will now pack the odu bits into the payload portion of the RS codes. This first RS code RS[0] is an RS(781,765) over m=10. Thus we need to pack 765x10 bits into the first 765 dectets of this code. Thus bits odu[0]...odu[9] form the first dectet of the first RS code. Bits odu[10]...odu[19] form the second dectet of RS[0]. The bits are repeatedly packed into 765 dectets of RS[0] for a total of 7650 bits, i.e. odu[0]...odu[7649]. At this point the data is then RS encoded over m=10 T=8, and 2T parity symbols are added to the code. Thus the next 16*10 bits consist of RS parity.

We will now consider the OTU output data. This consists of 16x255x4x8 bits or 130560 bits. We will number these bits otu[0]...otu[130559]. The first RS code is now mapped to the output otu. i.e. odu[0]...odu[7649] -> otu[0]...otu[7649]. The next 160 bits of rs parity are now mapped to the otu. i.e. rsparity[0]...rsparity[159] -> otu[7650]...otu[7809].

Having completed the first RS code, the next 7650 bits of odu are mapped to the otu. i.e. odu[7650]...odu[15299] -> otu[7810]...otu[15459]. These 765 dectets are rs encoded, and the 160

bits of rs parity are inserted into the outgoing otu. i.e. rsparity[0]...rsparity[159] -> otu[15460]...otu[15619].

This process is repeated for all 15 RS codes in the same manner. For the 16th and final code, there are 122368-15*765*10 = 7618 bits of remaining odu. These bits are packed into 762 dectets. The final 2 bits, which are missing are 0 filled and packed into the last dectet. These 762 dectets are RS encoded with an RS(778,762) code. Again 160 bits of parity are added to the outgoing otu. Thus odu[114749]...odu[122367] -> otu[117149]...otu[124767] . Note that the last 2 bits are 0 filled for the purpose of RS encoding, however they are not actually transmitted into the outgoing otu. The 160 parity bits are added as follows: rsparity[0]...rsparity[159] -> otu[124768]...otu[124927].

Having completed the RS outer code, the BCH inner code is now added to the otu. The 124928 otu bits are then mapped into 64 identical BCH codes of BCH(2040,1952) with m=11 and T=8, the parent code is shown above. This requires the 124928 bits to be grouped into 64 partitions of 1952 bits. The BCH mapping is as follows: otu[0] is used as the first bit for BCH[0]. otu[1] is used as the first bit for BCH[1] repeatedly until otu[63] is used as the first bit for BCH[63]. Then otu[64] is used as the second bit for BCH[0]. otu[65] is used as the second bit for BCH[1]. This process is repeated until all 124928 otu bits are consumed by the 64 BCH codes.

For each of the 64 BCH codes, the 1952 payload bits are encode and 88 parity bits are added to the output. The 88 bits result from the product of T=8 and m=11 for the BCH codes. The BCH parity is added to the output otu as follows:

BCH[0] bchparity[0] -> otu[124928], BCH[1] bchparity[0]-> otu[124929] repeatedly until BCH[63] bchparity[0]->otu[124992]. Then the next bit of each BCH code is added to the output otu. i.e. BCH[0] bchparity[1] ->otu[124993] This is repeated until all 64 BCH codes have exhausted their 88 parity bits. i.e.

BCH[63] bchparity[87] -> otu[130559] the last bit the output otu frame.

I.4.2.2 Reed-Solomon Encoder

The Primitive Binary Polynomial is as follows:

$p(x) = x^{10} + x^3 + 1$

I.4.2.3 BCH Encoder

The Primitive Binary Polynomial is as follows:

$p(x) = x^{11} + x^2 + 1$

I.4.3 Error Correction ability

Error Correction ability of this super FEC are shown in Table I.4 and in Figures I.13 and I.14.

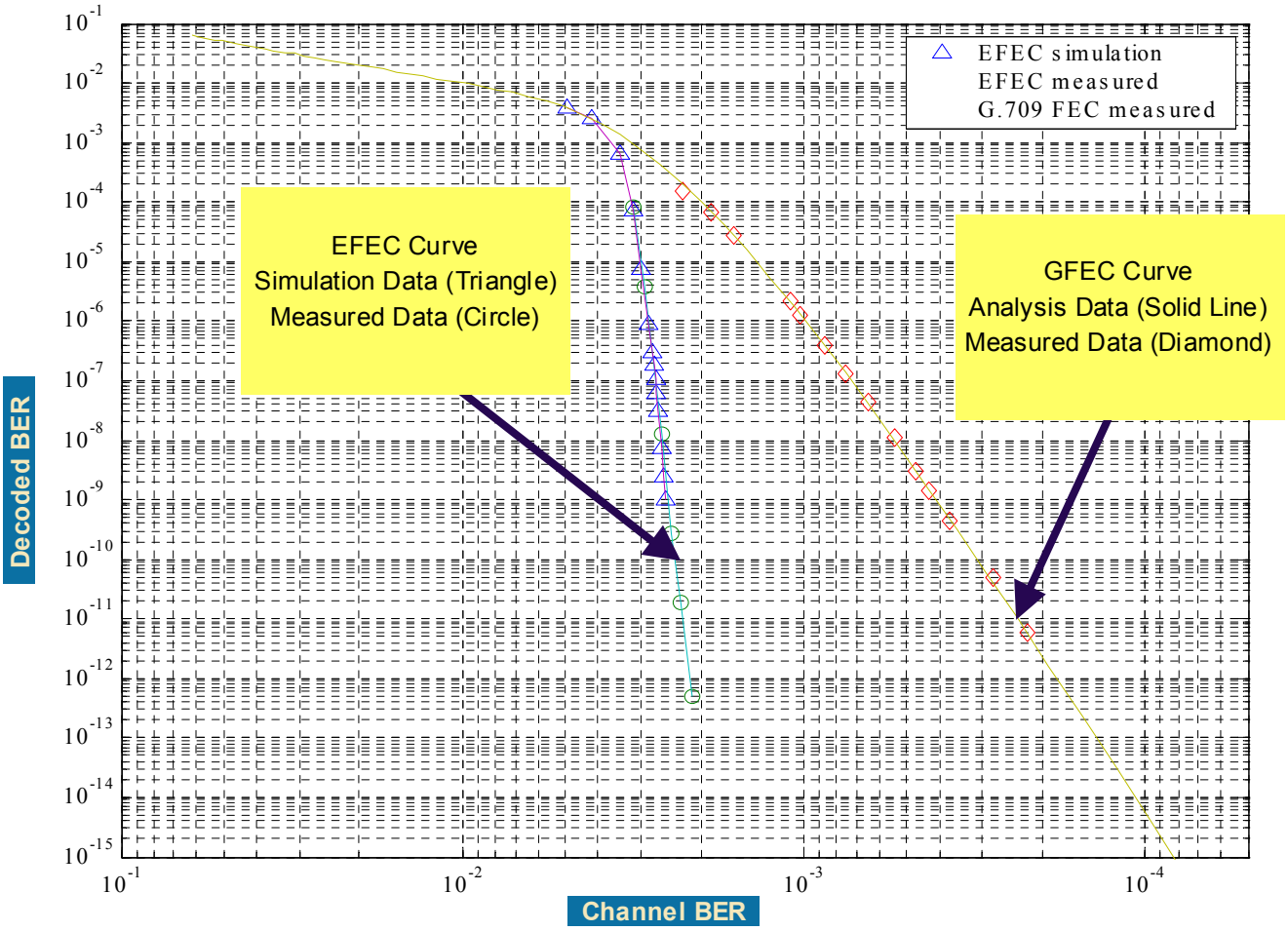

Figure I. 13/G.975.1 Results

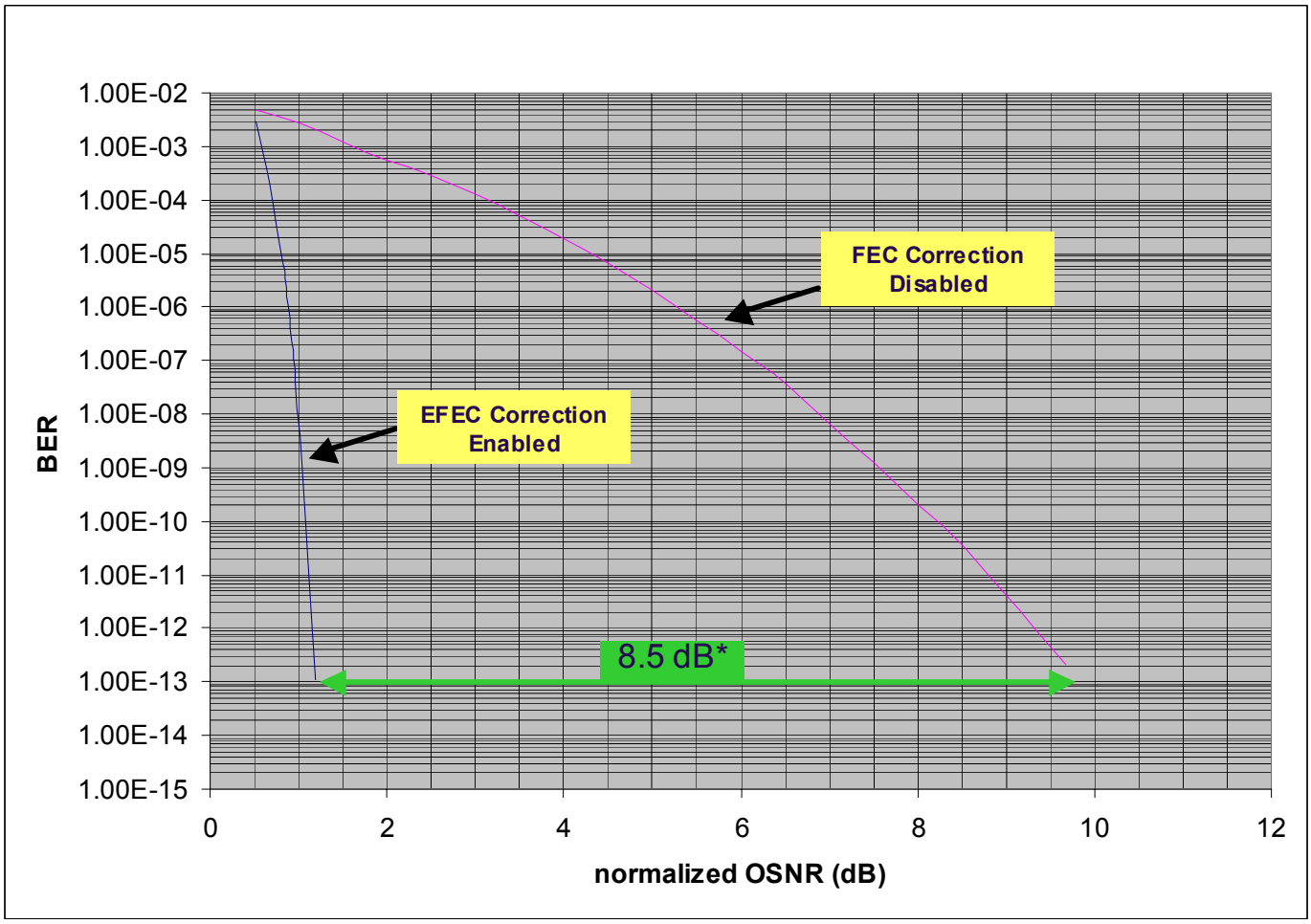

Figure I. 14/G.975.1 - Net Coding Gain

Table I. 4/G.975.1 - Summary for correction ability

Input BER	Output BER	Net coding gain (dB)	Coding gain (dB)	Q limit (dB)
2.41×10^{-3}	10^{-9}	6.31	6.59	9.0013
2.35×10^{-3}	10^{-10}	6.83	7.11	9.0262
2.30×10^{-3}	10^{-11}	7.30	7.58	9.0473
2.26×10^{-3}	10^{-12}	7.63	7.91	9.0645
2.23×10^{-3}	10^{-13}	8.03	8.31	9.0775
2.20×10^{-3}	10^{-14}	8.34	8.62	9.0906
2.17×10^{-3}	10^{-15}	8.67	8.95	9.1034

I.4.4 Redundancy Ratio

The redundancy ratio of the Interleaved RS(1023,1007)/BCH (2047,1952) Code is 7%, the same as the legacy RS FEC as defined in G.975

I.4.5 Latency

The latency is implementation dependent. Current implementations have been proven to have low latency.

I.4.6 Property

The code described provides excellent error correction capability over a broad range of operating conditions and channel error rates. The choice of the particular inner and outer codes, results in good performance being achieved in a small number of iterations (one or two) and results in a shorter latency as compared to many similarly performing codes which require a higher number of iterations. The choice of code also insures that no flaring in the performance curves will occur in the operating range of interest, (i.e. for BERs less than 10^{-20}).

I.5 Concatenated RS & Product Code Super-FEC scheme

I.5.1 Overview

This appendix describes a FEC code, which provides higher error correction capability than an RS(255,239) code, for exactly the same amount of overhead and which lends itself to soft decision decoding. Figure I. 15 shows an overview of this Super-FEC scheme. This Super-FEC scheme uses a concatenated code consisting of an Reed-Solomon RS(1901,1855) outer code and an Extended Hamming (512,502)×(510,500) Product inner code.

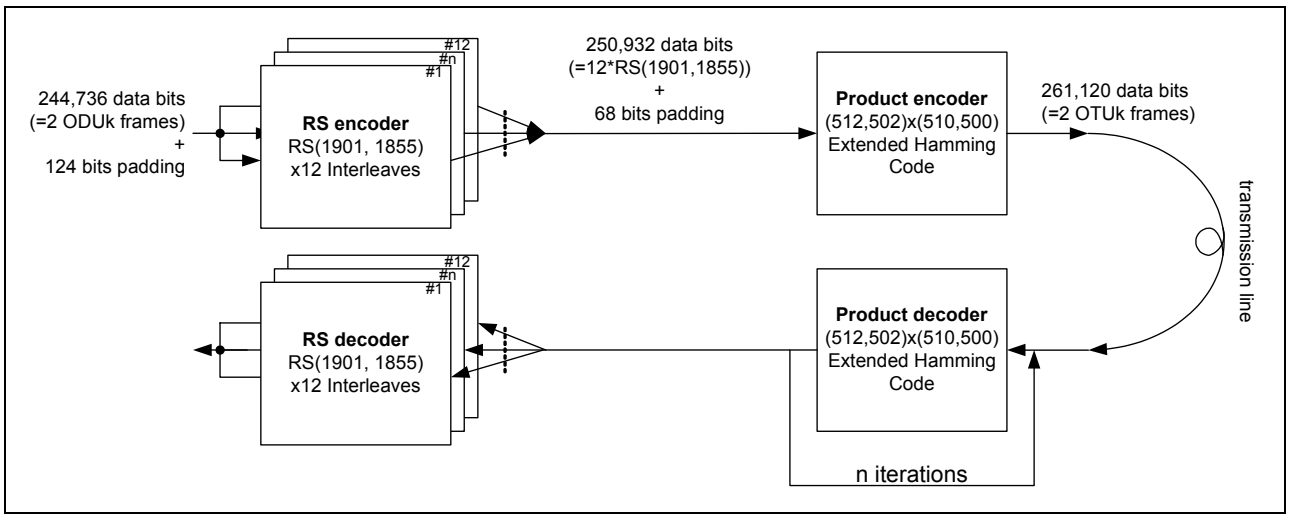

Figure I. 15/G.975.1 - Advanced-FEC scheme

I.5.2 Super-FEC algorithm

I.5.2.1 RS encoding

The outer RS code used is RS(1901,1855), with the generator polynomial given by:

$$G(z)=\prod_{i=0}^{45}\left(z-\alpha^{i+1001}\right)$$

where α is a root of the binary primitive polynomial $x^{11}+x^2+1$.

Elements of $GF(2^{11})$ are represented over the polynomial basis. The transmission order of the bits in a symbol is most significant bit first. The transmission order of symbols in a codeword is most significant symbol first, with the first 1855 symbols containing data and the remaining 46 symbols parity.

12 RS(1901,1855) codewords are interleaved, with the input payload data being distributed over these interleaves on a round-robin symbol-by-symbol basis.

124 bits are zero padded, as follows:

1) The least significant 3 bits of the last data symbol of the first interleave are zero padded

2) The last data symbols of the remaining 11 interleaves are zero padded

The total number of input data bits, for the 12 RS codes, is 244,736 (=11*12*1855-124). This is exactly the same as that for two ODU frames.

I.5.2.2 Product Code encoding

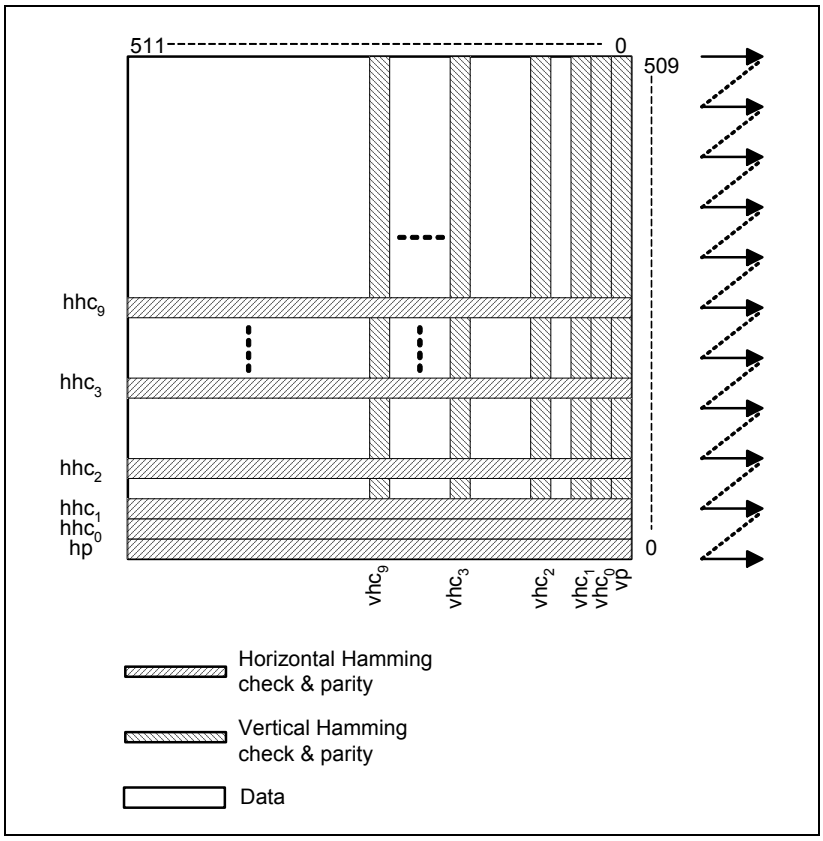

Figure I. 16/G.975.1 - Product Code matrix

In encoding a Product Code row the Hamming Check bits are arranged as follows: For the purpose of explanation we order the bits in each row from 511 down to 0, to designate the "position number" of each bit. Positions with power of 2 position number are occupied by Hamming check bits. Position 0 is occupied by the parity bit. The remaining 502 row positions are used for data.

The Hamming check bits are calculated by bit wise modulo-2 addition of the position numbers of all data bits with value "1". Hamming check bit 0 is located in position 1, Hamming check bit 1 in position 2, Hamming check bit 2 in position 4, etc. with the remaining Hamming check bits in positions 8, 16, 32, 64, 128 and 256.

Finally to form the parity bit, calculate the modulo-2 sum of all 511 Hamming codeword bits and assign the result to position 0.

The same principle applies to the coding of columns, but the code is shortened by removal of the bits with position numbers 511 and 510.

The resulting Product Code is therefore of length 512 x 510 = 261,120 encoded bits, which is exactly the same as two OTU frames.

After encoding the data as described, the Product Code matrix is transmitted on a row-by-row basis. The first bit to be transmitted is the bit from row 509 and column 511.

I.5.3 Error correction ability

The error correction ability of this Super-FEC code will depend upon the method of inner Product Code decoding (for example, upon the number of bits of quantization used by a soft decision decoder). Table I. 5 shows the error correction ability of a decoder using two bit (four levels) receiver quantization and performing 8 SISO iterations[1]. Table I.6 shows the error correction ability of the same decoder when used with a single bit (two levels) quantizer[1].

Table I. 5/G.975.1 - Summary for correction ability

Input BER	Output BER	Net coding gain (dB)	Coding gain (dB)	Q limit (dB)
4.7E-03	1.00E-09	7.0	7.3	8.3
4.7E-03	1.00E-10	7.5	7.8	8.3
4.7E-03	1.00E-11	7.9	8.2	8.3
4.6E-03	1.00E-12	8.4	8.6	8.3
4.6E-03	1.00E-13	8.7	9.0	8.3
4.6E-03	1.00E-14	9.1	9.3	8.3
4.5E-03	1.00E-15	9.4	9.7	8.3

[1] The coding gain values given are obtained by simulation and analysis.

Table I. 6/G.975.1 - Summary for correction ability

Input BER	Output BER	Net coding gain (dB)	Coding gain (dB)	Q limit (dB)
2.0E-03	1.00E-09	6.1	6.4	9.2
2.0E-03	1.00E-10	6.6	6.9	9.2
2.0E-03	1.00E-11	7.0	7.3	9.2
1.9E-03	1.00E-12	7.5	7.7	9.2
1.9E-03	1.00E-13	7.8	8.1	9.2
1.9E-03	1.00E-14	8.2	8.4	9.2
1.9E-03	1.00E-15	8.5	8.8	9.2

The burst error correction capability of this Super-FEC code will dependent upon the method of inner Product Code decoding, but will be at least 1024 bits.

I.5.4 Redundancy ratio

The redundancy ratio of this Super-FEC code is 6.69%, and is exactly the same as that of RS(255,239) code.

I.5.5 Latency

The latency associated with the encoding and decoding of this Super-FEC code is implementation dependent.

I.5.6 Properties

Iterative decoding can be applied to product codes. The Extended Hamming code is also amenable to soft decision decoding for enhanced coding gain. The proposed product code is thus suitable for soft-in-soft-out (SISO) iterative decoding. Further, the Extended Hamming code lends itself to soft decision decoding with modest decoding complexity (i.e. modest power dissipation). Soft decision receivers use 2 or more bit quantization, the number of bits used being vendor specific.

I.6 LDPC super FEC code

I.6.1 Overview

The code described here after is a systematic binary low-density parity-check (LDPC) code of length 32640, with 30592 information-carrying bits, identical to the length and dimension of the standard interleaved RS (255,239) code. This LDPC code is suitable for implementation in current chip technologies for 10G and 40G optical systems and has been shown to provide a significantly higher coding gain than the standardized RS code. The extra gain can for instance be used to improve the line parameters, the maximum span length, relax the optical component and line fibre specifications, or improve the overall quality of communication against degraded operation conditions.

I.6.2 Super FEC algorithm

The described FEC code is a systematic binary low-density parity-check (LDPC) code of length 32640, which is specified by a binary two-dimensional matrix *M* with 112 rows and 293 columns, the elements of which are indexed by the coordinates (*a*,*b*), where $0 \le a \le 111$ and $0 \le b \le 292$ as illustrated in Figure 1. This matrix, which contains a total of 32816 bits, is filled with 30592 information-carrying bits corresponding to a standard $239 \times 16 \times 8$ FEC frame payload as follows. The *j*th information bit, where $1 \le j \le 30592$, is located at coordinate $(r, 293r + 292 - q)$ in *M*, where $q = j + 172$ and $r = \lfloor q / 293 \rfloor$. The 173 entries (0,292-*d*), where $0 \le d \le 172$, are set to 'zero' and are not transmitted. It follows that the 30592 information-carrying bits are located in the first 105 rows, row 0 up to row 104 ($105 \times 293 - 173 = 30592$ bits). A total of 2051 parity-check equations determine the values of the last seven rows of *M* ($7 \times 293 = 2051$ bits) in the following manner. Consider the coordinates of the matrix *M* to form a grid of 112×293 points. A non-horizontal line through coordinate (0,*c*) with slope s_i, where $0 \le c \le 292$ and $0 \le s_i \le 292$, is defined as the set of coordinates $\{(a,b) \mid 0 \le a \le 111, b = (as_i + c) \bmod 293\}$, i.e., every non-horizontal line consists of exactly 112 points, seven of which are parity check positions. The code is now defined by selecting seven different slopes s_1, …, s_7, which, in turn, specify seven sets of 293 parallel lines through each point (0,*c*), where $0 \le c \le 292$. This implies that every coordinate (*a*,*b*) of *M*, where $0 \le a \le 111$ and $0 \le b \le 292$, is an element of seven lines of 112 elements each that intersect at coordinate (*a*,*b*). All code words of the LDPC code satisfy the condition that the parity check sum of the 112 bits specified by each of the $(7 \times 293) \cdot 7 = 2051$ lines is equal to 'zero' (using binary addition modulo 2). This completely defines the check bit values that are located in the last seven rows of *M*. The system of 2051 parity-check equations can be solved with $2051 - 6 = 2045$ parity-check bits and therefore there are 6 redundant check bits, which are chosen to be at positions (*v*,292), where $105 \le v \le 110$, as illustrated in Figure 1. These 6 positions are fixed to 'zero' and are not transmitted, i.e. only 2045 bits out of the 2048 available check bits per frame are used and transmitted. The mapping structure of the proposed systematic LDPC code of length 32640 with 30592 information-carrying bits and 2048 check bits is also illustrated in Figure 1. The LDPC code words have a format that is identical to the interleaved standard RS codes. The payload occupies the first $239 \times 16 \times 8$ bits, followed by three 'zeros' and the 2045 check bits. The check bit sequence corresponds to the sequence of elements (105,291), …, (105,0), (106,291), …, (106,0), (107,291), …, (107,0), (108,291), …, (108,0), (109,291), …, (109,0), (110,291), …, (110,0), (111,292), …, (111,0), i.e., a concatenation of the ((6×292)-bit rows 105 up to 110, followed by the 293 check bits of row 111. As previously indicated, the left-most elements (*v*,292), where $105 \le v \le 110$, corresponding to the redundant check bits that have been fixed to 'zero', are not transmitted and will be regenerated automatically in the decoder.

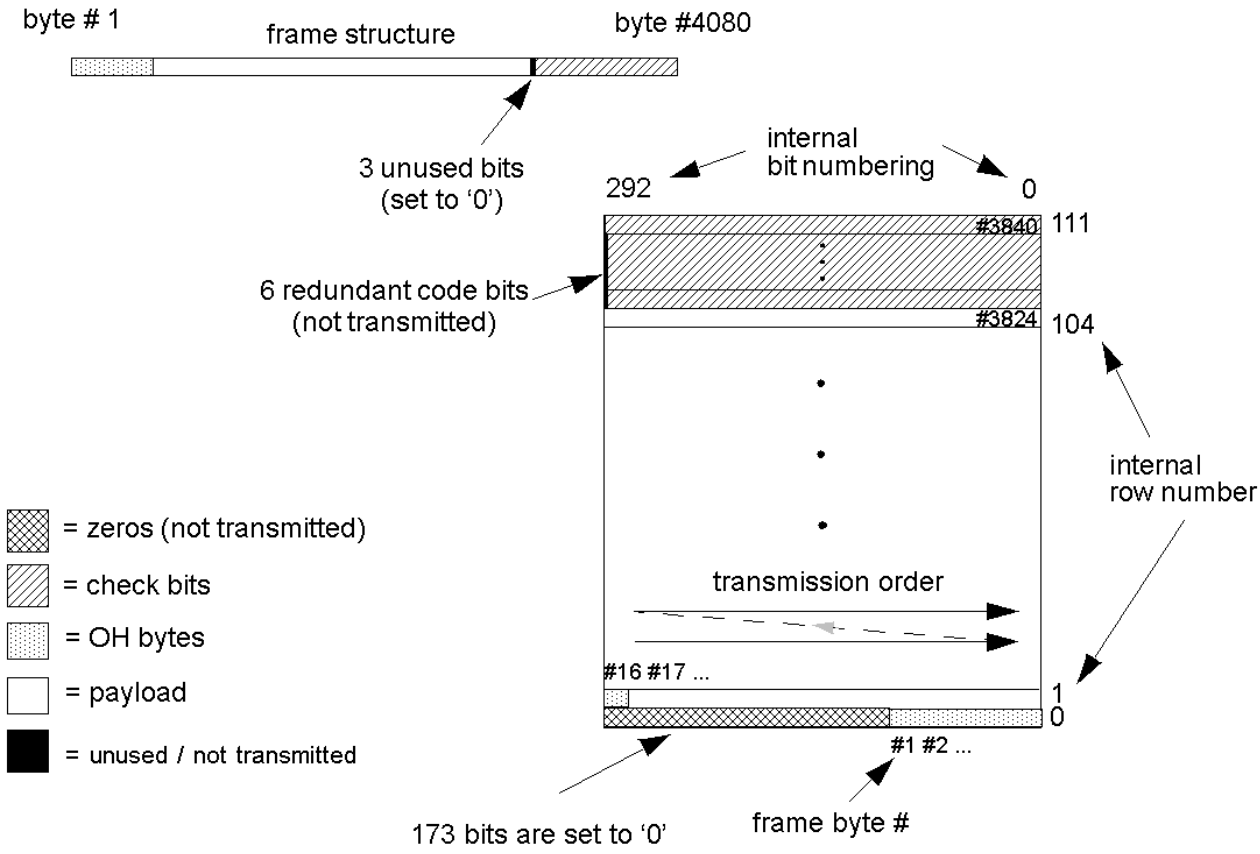

Figure I. 17/G.975.1 - Mapping structure for the LDPC code

The proposed code can be implemented efficiently with low power dissipation, which is of particular importance for 40G applications. Furthermore, there are powerful algorithms known for this code to exploit soft information, should this become available.

I.6.3 Error Correction ability

The performance of the LDPC code is shown in Figure I. 18 and Figure I. 19. The graphs have been obtained using a series of combined simulation and analysis techniques to accurately estimate the error performance for high and low input bit error rates. The actual measurements of an LDPC code implementation are in agreement with the simulations and confirm the accuracy of the estimation methods.

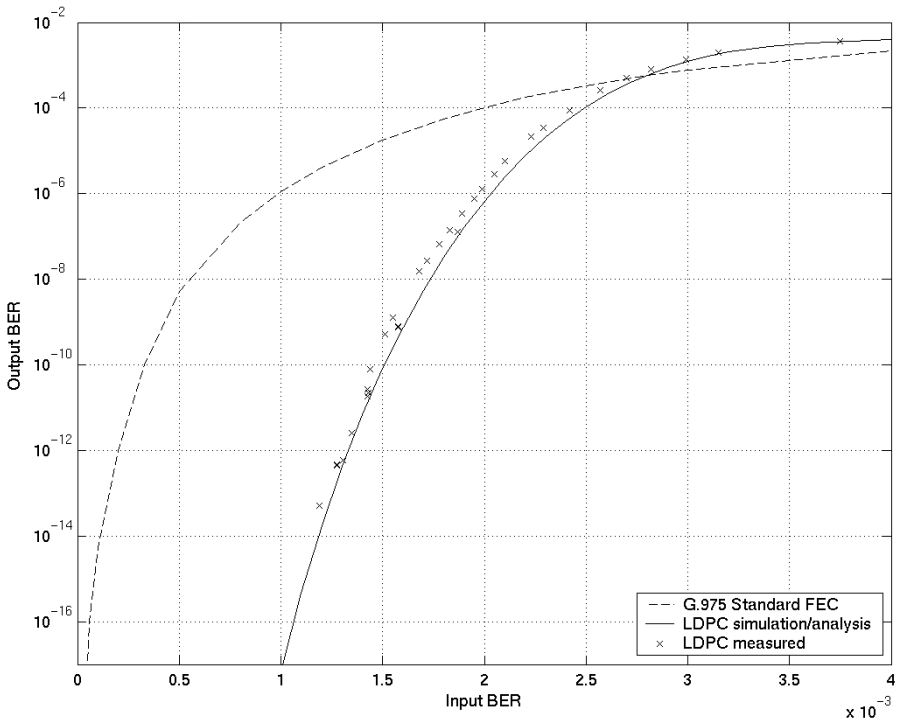

Figure I. 18/G.975.1 - Output BER as a function of the input BER for the LDPC code and for comparison the G.975 standard RS FEC code.

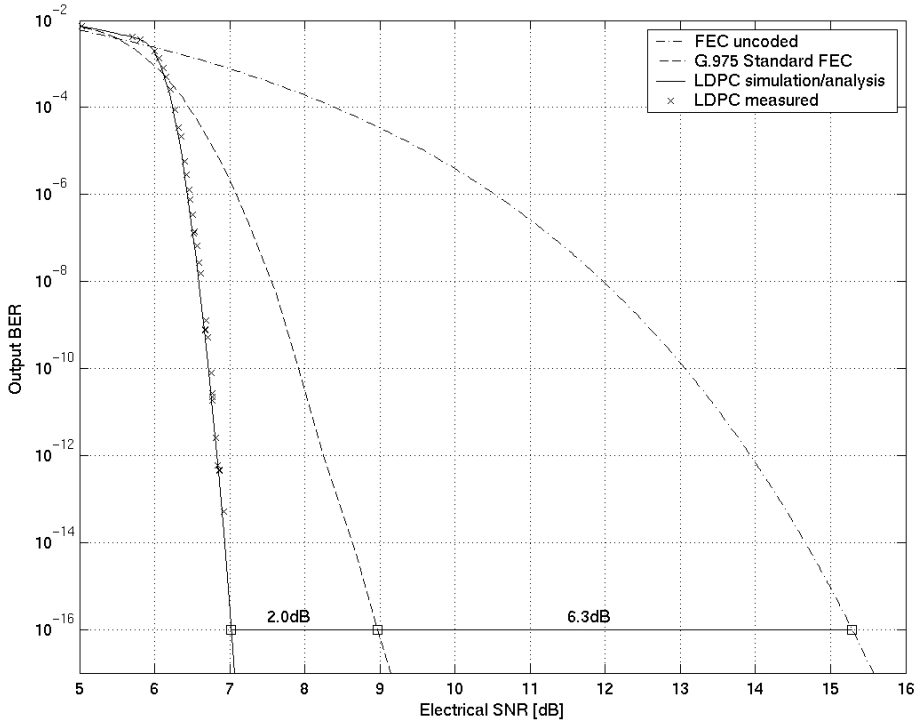

Figure I. 19/G.975.1 - Output BER as a function of the electrical SNR for the LDPC code and the existing standard RS FEC code.

Table I. 7/G.975.1 - Summary for correction ability

Input BER	Output BER	Net coding gain (dB)	Coding gain (dB)	Q limit (dB)
$1.61*10^{-3}$	10^{-9}	5.90	6.18	9.38
$1.51*10^{-3}$	10^{-10}	6.35	6.63	9.44
$1.42*10^{-3}$	10^{-11}	6.75	7.03	9.50
$1.33*10^{-3}$	10^{-12}	7.10	7.39	9.56
$1.25*10^{-3}$	10^{-13}	7.43	7.72	9.61
$1.18*10^{-3}$	10^{-14}	7.73	8.02	9.66
$1.12*10^{-3}$	10^{-15}	8.02	8.30	9.70

I.6.4 Redundancy ratio

The redundancy ratio of the LDPC strong FEC is with 7% the same as the legacy RS FEC as defined in G.975 and given by the relation of 32640 total transmitted bits, with 30592 information bits

I.6.5 Latency

The decoding latency of the described LDPC code can be implemented with low latency, as shown in Table I. 8 similar to the standard RS code.

Table I. 8/G.975.1 - Decoding latency of the LDPC code

Gbit/s	Latency [µs]
42.7	<3
10.7	~3
2.7	~12

I.6.6 Property

The described code is a systematic binary low-density parity-check (LDPC) code of length 32640, with 30592 information-carrying bits, identical to the length and dimension of the standard RS (255,239) code, as specified in the G.709 and G.975 recommendations. This LDPC code is suitable for implementation in current chip technologies for 10G and 40G optical systems offering low latency and feasibility of low power consumption in case of 40 G implementation showing a significantly higher coding gain than the standardized RS code.

I.7 Two orthogonally concatenated BCH super FEC code

I.7.1 Overview

This FEC scheme described hereafter will contain three parameterizations of the same scheme of two orthogonally interleaved block codes (BCH). The constructed code should be decoded iteratively, to achieve the expected performance. For practical reasons hard decision error correcting algorithms have to be implemented. The first option will apply for the special case of ITU-T G.709 compliant framing (7% overhead), while the two others will deliver a high performance option with 11% and 25% FEC overhead.

The performance of low overhead FEC algorithms, especially at low output error rates, heavily depends on the code word length. Though in general ITU-T G.975 allows any interleave and thus any frame size, especially in the case of frames compliant to ITU-T G.709 the frame length (130560 bits) imposes a major problem, if the code word length of the used FEC algorithm and the frame size are identical.

Thus, in opposite to other concepts, this scheme decouples the transmission framing from the structure used for FEC coding. Both are converted into each other using dedicated remapping schemes (see Figure I. 20). This scheme expects at the encoder incoming data to be formatted according to ITU-T G.975 (incl. scrambling) leaving the FEC overhead area void. This also allows using the same basic code system to be used for 25%, 11% and 7% overhead with remarkable performance in all cases.

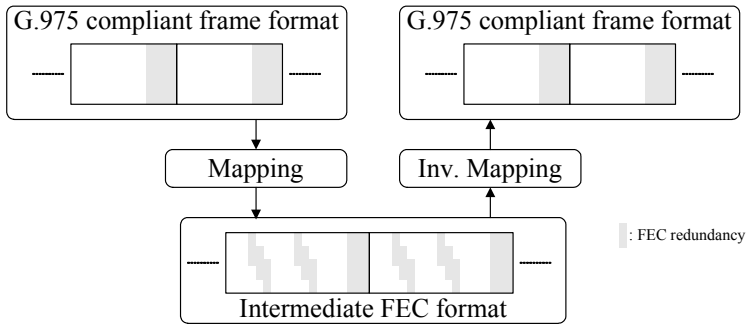

Figure I. 20/G.975.1 - Basic remapping scheme

In the following the underlying code system, the intermediate FEC format and the mapping into ITU-T G.975 compliant frames are described.

I.7.2 Super FEC algorithm

This section describes first the construction of the underlying code system of two orthogonally interleaved BCH codes. This is followed by the definition of the mapping procedure used of apply this coding scheme to the transmission stream.

I.7.2.1 Basic code system

The underlying code system consists of two orthogonally concatenated BCH code classes called "row encoding" and "column encoding". The corresponding code parameters are shown in Table I.9.

Table I. 9/G.975.1 - Basic code construction

Row Encoding	
Generator polynomials for t_r error correction code:	$G(x) = \prod_{i=1}^{2t_r-1} G_{2i-1}(x)$ $G_1(x) = x^{10}+x^3+1$ $G_3(x) = x^{10}+x^3+x^2+x+1$ $G_5(x) = x^{10}+x^8+x^3+x^2+1$ $G_7(x) = x^{10}+x^9+x^8+x^7+x^6+x^5+x^4+x^3+1$ $G_9(x) = x^{10}+x^7+x^5+x^3+x^2+x+1$ $G_{11}(x) = x^{10}+x^5+x^4+x^2+1$ $G_{13}(x) = x^{10}+x^6+x^5+x^3+x^2+x+1$ $G_{15}(x) = x^{10}+x^8+x^7+x^5+x^3+x+1$ $G_{17}(x) = x^{10}+x^9+x^8+x^6+x^3+x^2+1$ $G_{19}(x) = x^{10}+x^8+x^7+x^6+x^5+x^4+x^3+x+1$ $G_{21}(x) = x^{10}+x^9+x^8+x^7+x^6+x^5+x^3+x^+1$
Column Encoding	
Generator polynomials for t_c error correction code:	$G(x) = \prod_{i=1}^{2t_c-1} G_{2i-1}(x)$ $G_1(x) = x^9+x^4+1$ $G_3(x) = x^9+x^6+x^4+x^3+1$ $G_5(x) = x^9+x^8+x^5+x^4+1$ $G_7(x) = x^9+x^7+x^4+x^3+1$

Code words are processed in their natural order starting with the highest exponent, when considered as polynomials. When shortening the code word length the code word is padded with zeros starting at the highest exponent.

I.7.2.2 Intermediate FEC format

Conception wise, the basic BCH code words are used to construct a matrix of *x*y* bits (see left hand Figure I. 21). Each row consists of a single row code word of *x* bits. Each column represents a column code word of *y* bits. Two arbitrary row and column code words intersect in at most one bit.

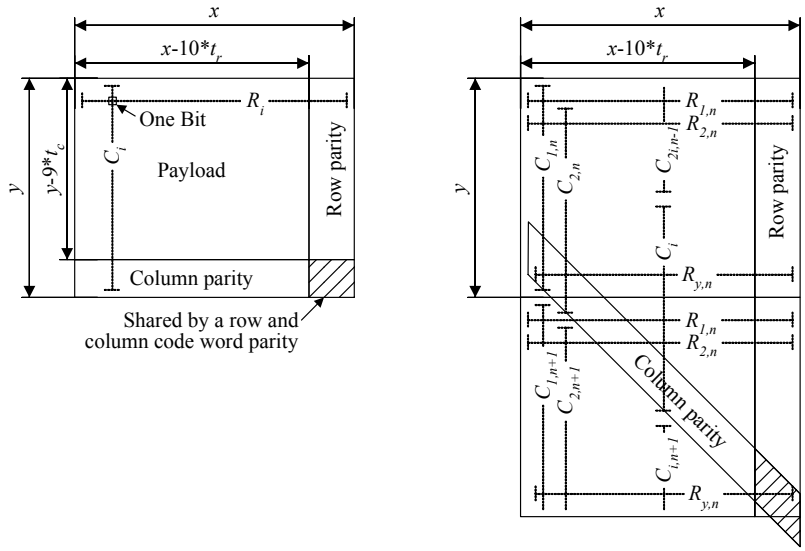

Figure I. 21/G.975.1 - Concept of orthogonally interleaved code words as matrix or streaming structure

The lower right hand quadrant (R/C) is shared between the two code classes. It is filled with parity of column code words computed over the row parity. Being linear algebraic codes, this is identical to the parity of row code words computed over the column code word parity. Thus, in this matrix representation, it would only be needed to be computed and transmitted once. The size of this matrix depends on the precise code parameters. In the described configurations it is in the range of ~500kBit.

To ease implementation, this matrix structure is reformatted into a streaming structure, which is concept wise shown right hand of Figure I. 21. It shows that the column words are now no longer aligned against the matrix boundaries, but are shifted across more than two matrices in case $y'<y$. Here the modified matrix has a fixed logical width of 32-bits ($y'=32$).

In Figure I. 22 the allocation of the row code words ($R_{i,m}$) into the stream of modified matrices is shown. 32 independent code words of length X are mapped to a set of 32 adjacent bits, so they are bit wise interleaved. They form a code word group R_m with all 32 code words aligned to the same set of 32 adjacent bits.

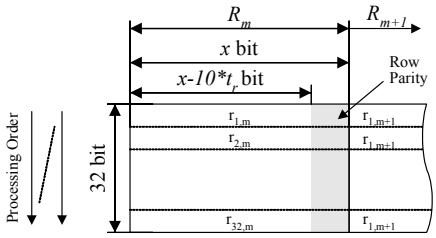

Figure I. 22/G.975.1 - Row code allocation

The column code words are mapped vertically over this structure as shown in Figure I. 23.

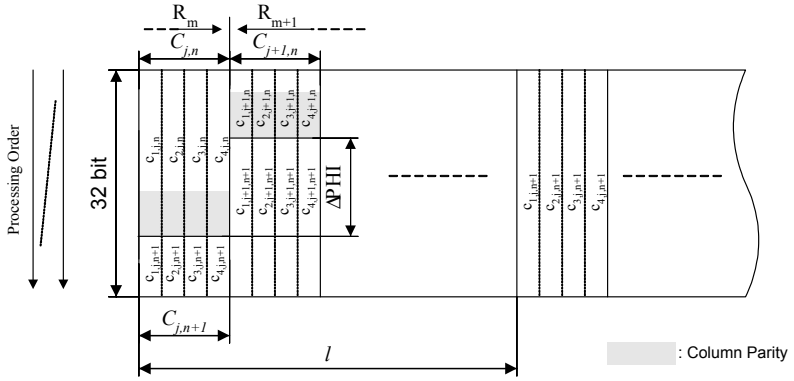

Figure I. 23/G.975.1 - General Mapping of column code words over the data stream

Each 32-bit column is either member of a single column code word $c_{a,b,d}$ (a: index within a column group, b: column group index, d: time sequential index) or, in case of a code word boundary within a 32-bit column, of the two column code words $c_{a,b,d}$ and $c_{a,b,d+1}$. Four adjacent columns form a column group ($C_{b,d}$). Each code word of this group starts with the same code word bit index $PHI_{b,d}$ in row one. Thus the code word boundaries of all column code words of a group are aligned to the same row index. The following code word group (either $C_{b+1,d}$ *or* $C_{1,d+1}$) has an allocation shifted by ΔPHI bits ($PHI_{1,d+1}$, $PHI_{b+1,d}$= ($PHI_{b,d}$ +ΔPHI) mod y). A group is never spread over two row code word groups ($R_{i,m}$, $R_{i,m+1}$). Thus, the row code word length must be a multiple of 4. The column code bit index is incremented by d for each consecutive group. A total of l of such column groups exist ($0<b\leq l$; $4*l \geq x$).

The resulting column code word mapping is unrelated to the row code word allocation except that a column code word group never spans over two adjacent row code word groups ($R_{i,m}$, $R_{i,m+1}$). Thus it may happen that certain column code word groups want to place their redundancy in the area of row code redundancy of row code word group R_m. This corresponds to the collision situation in the quadrant R/C of the matrix representation shown in Figure I. 21. As the mapping is no longer algebraic, this has to be resolved by separate transmission of the column code parity. To reach this, the set of n column code word groups $C_{j(i),d}$ ($j(i)<j(i+1)$, $0<j(i)\leq l$,$0<i\leq n$), which would produce this collisions, are removed from the sequence of column code word groups generated by shifting the column code word boundaries by ΔPHI. The removed column code word groups are reinserted at the beginning of the next row code word group R_{m+1} in the order they were removed. In Figure I. 24 the example of four column code word groups swapped is shown.

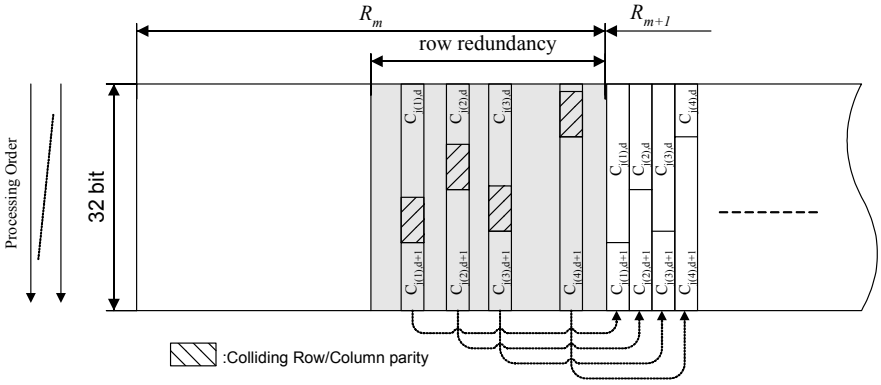

Figure I. 24/G.975.1 - Example of shifting four column code word groups

After reinsertion of the removed column code word groups, the code word alignment is continued in accordance to the unmodified original sequence.

Being a non-algebraic structure, is further required to define to correct order of encoding. Here, first the column code word coding is applied to the data stream, which is then followed by the row encoding.

I.7.2.3 Mapping from G.975 compliant framing into internal representation

For all overhead rates the same basic ITU-T G.975 compliant framing structure is used as shown in Figure I. 25.

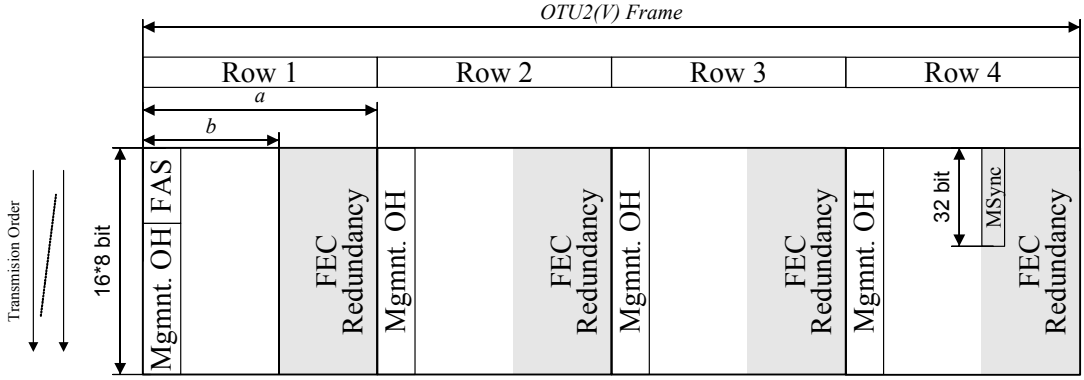

Figure I. 25/G.975.1 - Used ITU-T G.975 compliant framing

It consists of 128 1-bit wide rows. Each row has a length of *a* bits, of which *b* bits are used as payload and management overhead and *(a-b)* bits as FEC redundancy space. An OTU2(v) frame is build by concatenating four of the described frames. Each frame represents a single row of the OTU2(v) framing. The exact parameterization is shown in Table I. 10.

Table I. 10/G.975.1 - Parameterization of the transmitted framing

	a	***b***	**Code rate D_f**
ITU-T G.709 compliant OTU*k* framing	32640 bit	30592 bit	239/255
ITUT G.709 compliant OTU*k*V framing (11% mode)	33536 bit	30592 bit	239/262
ITUT G.709 compliant OTU*k*V framing (25% mode)	38016 bit	30592 bit	239/297

The frame representing the fourth OTU2(V) row also contains a 32-bit wide field at the beginning of the FEC redundancy portion used to synchronizes the following mapping procedure.

I.7.2.3.1 Mapping procedure

The mapping process consists of two functions. First the G.975 compliant frame is disassembling into the payload information (incl. OXU*k*(V) management overhead) and FEC redundancy bits. Both are written into two separate FIFO stores in the order received (see Figure I. 26) except for the MSync pattern, which is discarded from the data stream.

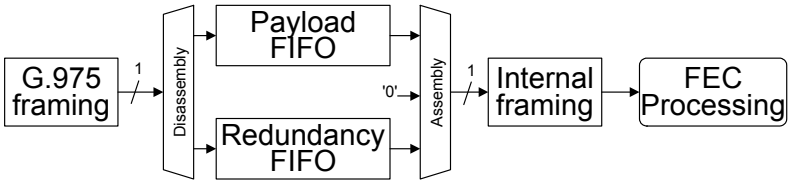

Figure I. 26/G.975.1 - Basic reformatting flow

In a second step, data is read out of the FIFO stores to form the internal framing. Of each column code word group the first row bits of each code word are filled in the sequential order. Then the next row is filled. After completion of a column code word group the next group is assembled. This process is shown in Figure I. 27. The numbers at the single bit locations represent the time order in which they are assembled.

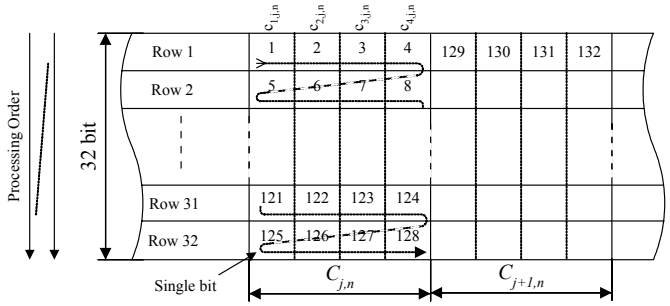

Figure I. 27/G.975.1 - Basic mapping to internal framing

For the 25% OH mode, one column code word group ($C_{k,n}$) is filled with row parity by half (see Figure I. 28). For this group the assembly order is modified that each column code word is filled completely before the next is assembled.

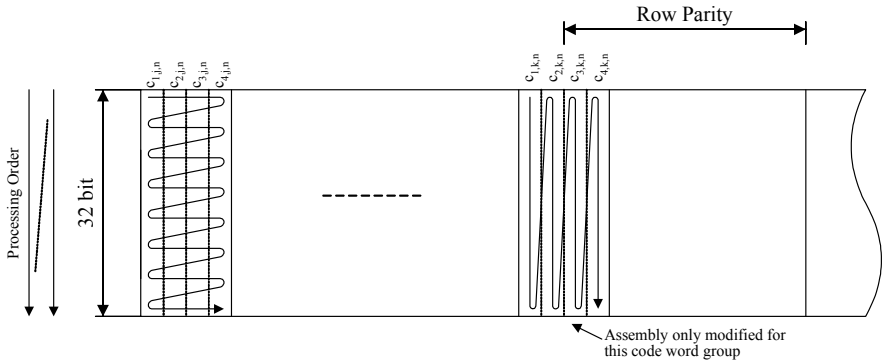

Figure I. 28/G.975.1 - Mapping for the 25% mode

Depending on the type of information required, either the payload data FIFO or the redundancy FIFO is read out to fill the bit positions. Additionally the 32-bit wide mapping synchronization pattern (MSync) is replaced by a string of zeros.

I.7.2.3.2 Rate adaptation

To compute the internal FEC rate D_f it is assumed that the interleaving between row and column code words is altered in a way that both code words fully overlap. This also requires the column code word to be scaled by x/y as seen in Figure I. 29.

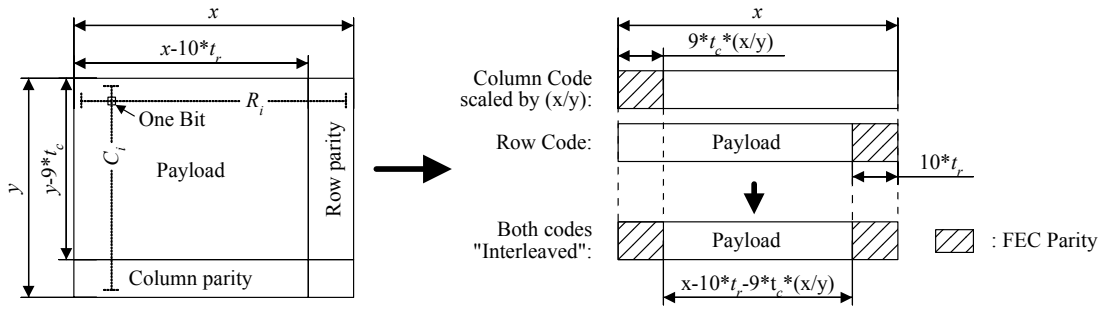

Figure I. 29/G.975.1 - Simplification of interleave to support rate computation

The resulting internal FEC overhead rate D_f is then given by:

$$D_f = \frac{x - 10t_r - 9\frac{x}{y}t_c}{x} = 1 - 10\frac{t_r}{x} - 9\frac{t_c}{y}$$

For feasible mappings D_f must be greater than the code rate D_c determined by the OTU*k*(V) mapping as seen in Table I. 11.

Table I. 11/G.975.1 - Raw FEC rate vs. OTU(v) rate

	D_f	D_c	D_c'
ITU-T G.709 compliant OTU*k* framing	4219/4500≈0.9375	239/255≈0.9372	≈0.9381
ITU-T G.709 compliant OTU*k*V framing (11% mode)	7447/8160≈0.91262	239/262≈0.91221	≈0.91308
ITU-T G.709 compliant OTU*k*V framing (25% mode)	3588/4420≈0.8049	239/297≈0.8047	≈0.8053

The adaptation is performed by first increasing D_c to D_c' by removing the 32 bits of MSync pattern when writing OTU*k*V data into the mapping FIFOs.

In a second step for each internal row code word group R_m a dedicated column code word group C_a is selected to implement the rate adaptation. By default, this is the 10th column code word group after start of R_m. In cases where this column code word group contains column parity, the 9th group is selected instead.

At the beginning of the third column code word group before C_a (7th or 6th column code word group of R_m), the fillings of the data FIFO (DFILL) and the Parity FIFO (PFILL) are checked against fixed limits (see Table I. 12 through Table I. 14). Depending on the result of this comparison, C_a is assembled from variable portions of bits from the data FIFO, the parity FIFO. Unused space is filled with zeros. Note that, yet data is pulled from the parity FIFO, it is always considered as data by the subsequent FEC decoder.

Using the bit numbering within the column code word group as defined in Figure I. 27, C_a is assembled as shown in Figure I. 30.

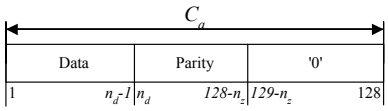

Figure I. 30/G.975.1 - Data allocation within C_a

Table I. 12/G.975.1 - Rate adjustment rules for 7% OH setting (OTUk framing)

Condition		n_d	n_z
DFILL > 7168	PFILL > 768	104	24
DFILL > 7168	PFILL < 768	96	24
DFILL < 7168	PFILL > 768	88	40
DFILL > 7168	PFILL > 768	80	40

Table I. 13/G.975.1 - Rate adjustment rules for 11% OH setting (OTUkV framing)

Condition		n_d	n_z
DFILL>8832	PFILL >4480	88	24
DFILL >8832	PFILL <4480	80	24
DFILL <8832	PFILL>4480	72	40
DFILL >8832	PFILL>4480	64	40

Table I. 14/G.975.1 - Rate adjustment rules for 25% OH setting (OTUkV framing)

Condition		n_d	n_z
DFILL>11136	PFILL >6400	112	16
DFILL >11136	PFILL <6400	104	16
DFILL <11136	PFILL>6400	96	32
DFILL >11136	PFILL>6400	88	32

I.7.2.3.3 Mapping Synchronization

To synchronize the internal format between the sending encoder and the receiving decoder, a 32-bit wide pattern (MSync, see Figure I. 25) is used. This pattern is replaced by a zero string before mapping. It conveys the following information in two alternatively inserted MSync pattern (see Figure I. 31):

Table I. 15/G.975.1 - Transmitted synchronization information

Name	**Size**	**Initialization latency *u* in bit (see** Figure I. 32**)**			**Function**
		7% OH	**25% OH**	**11% OH**	
IX	9 bit	2400	7776	3040	Sets the row code to process the IXth bit of code word (initializes the row code word allocation shown in Figure I. 22)
PHI	9 bit	2400	7776	3040	Sets the column code word bit to PHI (initializes the column code word allocation shown in Figure I. 23)
PHIS	3 bit	2400	7776	3040	The number of currently removed column code words before the column code word being initialized by PHI
DFILL	14 bit	2656	8032	3296	Sets the filling of the data FIFO to DFILL
PFILL	14 bit	2656	8032	3296	Sets the filling of the parity FIFO to PFILL

The five quantities are split over two MSync pattern transmitted alternatively in two consecutive OTU*k*(v) frames. The allocations are shown in Figure I. 31.

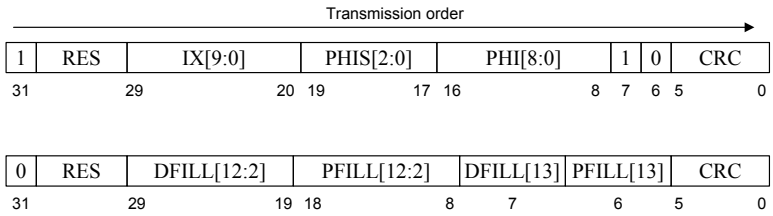

Figure I. 31/G.975.1 - Structure of the mapping synchronization pattern

Both pattern are protected using a 6-bit CRC added to the 24 information bits MSync[29:6]. The check matrix is given by:

$$CRC[5:0] = \begin{bmatrix} 1&1&0&0&0&1&1&0&1&1&1&0&0&1&0&1&0&0&0&1&0&0&0&0 \\ 0&1&1&0&0&0&0&1&0&0&0&1&0&0&1&0&1&0&0&1&1&0&0&0 \\ 0&1&1&1&0&1&0&0&0&0&0&0&1&0&0&1&0&1&0&0&1&1&0&0 \\ 1&0&1&1&1&0&1&0&0&0&1&0&0&0&0&0&1&0&1&0&0&1&1&0 \\ 0&0&0&1&1&0&1&1&1&0&0&1&0&1&0&0&0&1&0&0&0&0&1&1 \\ 1&0&0&0&1&1&0&1&1&1&0&0&1&0&1&0&0&0&1&0&0&0&0&1 \end{bmatrix} MSync[29:6]$$

The extracted information is executed *u* bits after reception of the last bit of the sync pattern containing the FIFO fill settings (PFILL,DFILL).

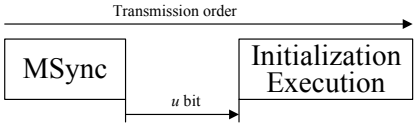

Figure I. 32/G.975.1 - Latency of initialization

I.7.2.3.4 Mode Configurations

A summary of the parameterization of the two defined modes is shown in Table I. 16.

Table I. 16/G.975.1 - Configuration summary

Description		Symbol	7% Mode	11% Mode	25% Mode
transport framing row length		*a*	32640 bit	33536 bit	38016 bit
payload length		*b*	30592 bit	30592 bit	30592 bit
Code Rate		-	239/255	239/262	239/297
OTU1(V) / STM-16		-	255/238 ≈ 1.0714	262/238 ≈ 1.1001	297/238 ≈1.2479
OTU2(V) / STM-64		-	255/237 ≈ 1.0759	255/237 ≈ 1.1054	297/237 ≈1.2531
OTU3(V) / STM-256		-	255/236 ≈ 1.0805	255/236 ≈ 1.1101	297/236 ≈1.2584
Row code:	Code Word length	*x*	900	960	884
	Correctable bits per code word	t_r	4	5	11
Col. code:	Code Word length	*y*	500	510	510
	Correctable bits per code word	t_c	1	2	4
Number of column code word groups		*l*	286	262	262
Column code word shift		ΔPHI	286	296	296

I.7.3 Error correction capability

Based on the terms and definitions given in section 7, Table I. 17 - Table I. 19 show the results for the three different configurations. Non-shaded rows contain measured data, while shaded rows contain extrapolated data based on simulations. It is assumed the stream is decoded iteratively using the five steps each implementing a hard decision BCH decoder as shown in Figure I. 33. Different decoding strategies will deliver different performance.

Figure I. 33/G.975.1 - Five step iterative decoding

Table I. 17/G.975.1 - Error correcting capability of the 7% OH setting

Input BER	Output BER	Net coding gain (dB)	Coding gain (dB)	Q limit (dB)
$2.700*10^{-3}$	10^{-9}	6.35	6.67	8.89
$2.550*10^{-3}$	10^{-10}	6.80	7.12	8.95
$2.400*10^{-3}$	10^{-11}	7.20	7.52	9.01
$2.200*10^{-3}$	10^{-12}	7.53	7.85	9.09
$2.000*10^{-3}$	10^{-13}	7.82	8.14	9.18
$1.62*10^{-3}$	10^{-14}	7.98	8.29	9.38
$1.30*10^{-3}$	10^{-15}	8.09	8.41	9.58

Table I. 18/G.975.1 - Error correcting capability of the 11% OH setting

Input BER	Output BER	Net coding gain (dB)	Coding gain (dB)	Q limit (dB)
$4.920*10^{-3}$	10^{-9}	6.89	7.32	8.24
$4.850*10^{-3}$	10^{-10}	7.38	7.81	8.26
$4.740*10^{-3}$	10^{-11}	7.81	8.25	8.28
$4.630*10^{-3}$	10^{-12}	8.20	8.64	8.31
$4.580*10^{-3}$	10^{-13}	8.57	9.01	8.32
$4.50*10^{-3}$	10^{-14}	8.90	9.33	8.34
$4.44*10^{-3}$	10^{-15}	9.19	9.63	8.36

Table I. 19/G.975.1 - Error correcting capability of the 25% OH setting

Input BER	Output BER	Net coding gain (dB)	Coding gain (dB)	Q limit (dB)
$1.340*10^{-2}$	10^{-9}	7.68	8.66	6.90
$1.330*10^{-2}$	10^{-10}	8.17	9.15	6.91
$1.323*10^{-2}$	10^{-11}	8.63	9.61	6.92
$1.320*10^{-2}$	10^{-12}	9.04	10.02	6.93
$1.312*10^{-2}$	10^{-13}	9.41	10.39	6.93
$1.307*10^{-2}$	10^{-14}	9.75	10.73	6.94
$1.302*10^{-2}$	10^{-15}	10.06	11.04	6.95

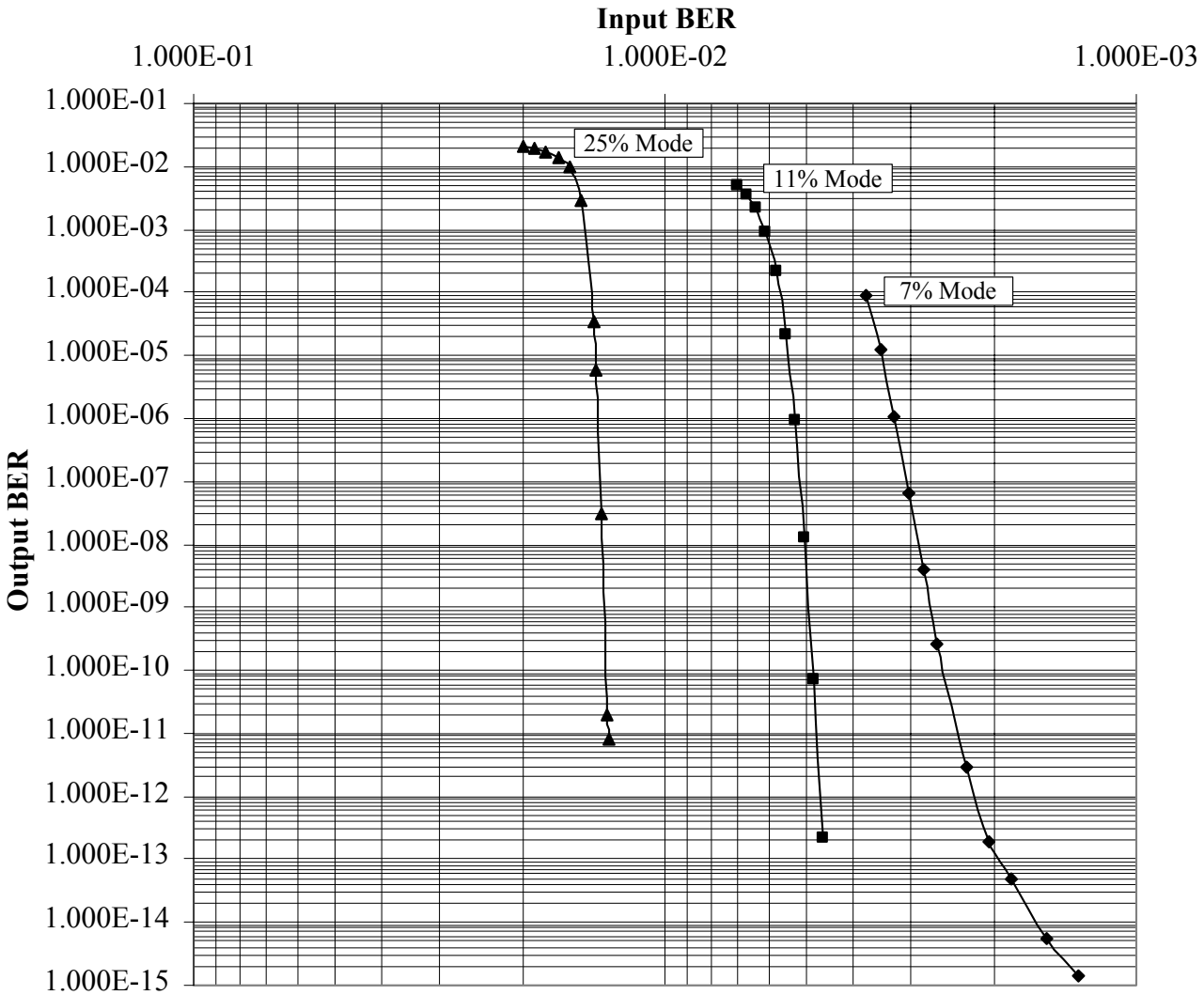

Figure I. 34/G.975.1 - FEC performance Input BER vs. Output BER

I.7.4 Redundancy ratio

In Table I. 20 the FEC redundancy ratios and the net rate ratios resulting from different mapping according to ITU-T G.709 are shown. Note that mapping STM-64 into OTU2(V) and STM-256 into OTU3(V) imply introduction of unused fixed stuff columns, further increasing the overall rate.

	7% OH mode	11% OH mode	25% OH mode
Redundancy ratio	255/239 ≈ 1.066	262/239 ≈ 1.096	297/239 ≈ 1.2426
OTU*k*(V) / CBR	255/238 ≈ 1.0714	262/238 ≈ 1.1001	297/238 ≈1.2479
OTU1(V) / STM-16	255/238 ≈ 1.0714	262/238 ≈ 1.1001	297/238 ≈1.2479
OTU2(V) / STM-64	255/237 ≈ 1.0759	255/237 ≈ 1.1054	297/237 ≈1.2531
OTU3(V) / STM-256	255/236 ≈ 1.0805	255/236 ≈ 1.1101	297/236 ≈1.2584

Table I. 20/G.975.1 - Redundancy ratios for different mapping

I.7.5 Latency

The latency depends on the selected implementation as well as on the number of iterations performed while decoding. However, there is a lower bound of ~500 Kbit per column code word processing stage. Thus the decoding strategy described in I.7.3 will lead to a latency of ~ 1MBit. In case of 10Gbit/s payloads (STM-64, ODU2) this will result in 100µs delay.

I.7.6 Properties

The described scheme provides strong error correction capabilities over a wide range of code rates, while showing no or only very limited flaring. It does not rely on soft decision algorithms for decoding. The overall introduced latency is moderate.

I.8 Reed Solomon (2720,2550) super FEC Code

I.8.1 Overview

Modern high-speed optical transmission systems rely heavily on forward error correction (FEC) to provide quasi error-free transmission over optical channels. The G.975 recommendation underlying specifies the standard RS (255,239) codes with 8-bit symbols, interleaved with depth 16, as the default FEC code for optical transmission systems. This interleaved FEC code is a systematic block code of length 32640 with 30592 information-carrying bits. It can correct up to eight symbol errors in each of the 16 interleaved streams of 2040 bits. .

I.8.2 Super FEC Algorithm

A Reed Solomon code of length N over Galois Field GF(q) is a cyclic code with generator polynomial

$$g(x) = (x - \alpha^b)(x - \alpha^{b+1}) \cdots (x - \alpha^{b+D-2})$$

where α is a primitive element of GF(q), D is the minimum distance, $K = N - D + 1$ is the dimension and b is an arbitrary offset [2], [3]. This code, referred to as an RS (N,K) code, can correct up to $t = \lfloor (D-1)/2 \rfloor = \lfloor (N-K)/2 \rfloor$ symbol errors, where $\lfloor a \rfloor$ denotes the largest integer smaller than or equal to a. For practical purposes, we consider the class of RS codes over GF(2^m), the elements of which can be represented by binary m-tuples, to form an RS (n=mN,k=mK) code over GF(2).

Let n_b denote the total block length of the frame. For $n_b > mN$, it is common to interleave the symbols of the RS (N,K) codes to provide a high burst error correction capability, or, preferably to increase the error correction parameter t and maintain the same overhead by increasing the block length n, where $n \le m(2^m - 1)$ and therefore increasing m. The interleaving depth is consequently reduced to $u \le \lfloor n_b / m(2^m - 1) \rfloor$ and $N = \lceil n_b / mu \rceil$, where $\lceil a \rceil$ denotes the smallest integer larger than or equal to a.

Let $B_{\max}$ denote the maximum burst error length that can always be corrected. It is easy to verify that the burst error capability of an RS (N,K) code over GF(2^m) with interleaving depth u is given by $B_{\max} = u \cdot t$. However, a more relevant parameter is the guaranteed burst error capability in the presence of random errors. The maximum burst error length $B_{\max}^{(v)}$ in the presence of v random errors can be expressed by

$$B_{\max}^{(v)} = \max(0, t - v) \cdot u \quad [m\text{-bit symbols}]$$

The burst error length in bits, $b_{\max}^{(v)}$, is consequently given by

$$b_{\max}^{(v)} = \max(0, mB_{\max}^{(v)} - (m-1)) \quad [\text{bits}]$$

where the non-alignment of the beginning and end of the burst error and the m-bit symbols has been taken into account.

The error correcting capability of a bounded distance decoder is exceeded if $e > t$ symbol errors occur. The word error probability $P_w^{(n)}$ at the output of a bounded distance RS $(n = mN, k = mK)$ decoder after transmission over a binary symmetric channel with a bit error probability p_b is therefore given by

$$P_w^{(n)} = \sum_{e=t+1}^{N} \binom{N}{e} p_s^e (1 - p_s)^{N-e}$$

where $p_s = 1 - (1 - p_b)^m$ is the symbol error probability. For an interleaved RS (N,K) code, the expression for the word error probability becomes

$$P_w^{(u \cdot n)} = 1 - (1 - P_w^{(n)})^u$$

If the transmitted codeword has $e > t$ symbol errors, the decoder will either fail to find a codeword (decoder failure), or it will find a codeword other than the transmitted codeword (decoder error). It has been shown in [4] that the decoder error probability is less than $1/(t!)$. In the case of a decoder failure, the decoder will leave the received word unchanged, which effectively means that the number of symbol errors equals e and the average number of bit errors equals $e \cdot mp_b / p_s$. In the case of a decoder error up to t extra random errors will be added, in which case the average number

of bit errors equals $e \cdot mp_b / p_s + t \cdot m/2$. It follows that the bit error probability P_b can now be accurately approximated by

$$P_b \cong \frac{1}{N} \sum_{e=t+1}^{N} \left(\frac{p_b}{p_s} \cdot e + \frac{1}{2(t-1)!} \right) \binom{N}{e} p_s^e (1-p_s)^{N-e}$$

The following paragraph uses the derived expressions implicitly to obtain the parameters of the RS code and to determine its performance.

The proposed FEC code is an RS (2720,2550) code with 12-bit symbols and a total length of 32640 bits. The polynomial that generates the elements over Galois Field GF(2^{12}) is given by

$$p(x) = x^{12} + x^9 + x^8 + x^6 + x^3 + x^2 + 1.$$

This code supports up to 30600 information-carrying bits. The first 30588 bits of the standard $239 \times 16 \times 8$ FEC frame payload will be mapped onto the first 2549 symbols. The last four bits of the payload will form the four most significant bits of the 2550th symbol and the remaining 8 bits of this symbol are unused. They can either be specified or set to zero.

I.8.3 Error Correction ability

The RS (2720,2550) code can correct up to 85 symbol errors, and the bit error rate at the decoder output can therefore be easily determined. The results are shown in Figures I. 35 and 36 and in Table I. 21. It is clear that the low minimum distance of the RS (255,239) code, that is only able to correct up to 8 symbols in one of the interleaved 2040 bits blocks, has a severe impact on the error correction performance of the standard FEC code. The maximum burst error correction capability $b_{\max}^{(v)}$ of the RS (2720,2550) code is given by $\max(0,12 \cdot (85 - v) - 11)$ in the presence of v additional random errors. As a comparison, the interleaved RS (255,239) code is capable of correcting $\max(0,128 \cdot (8 - v) - 7)$. This illustrates that the burst error correction capability of the latter is much more susceptible to random errors.

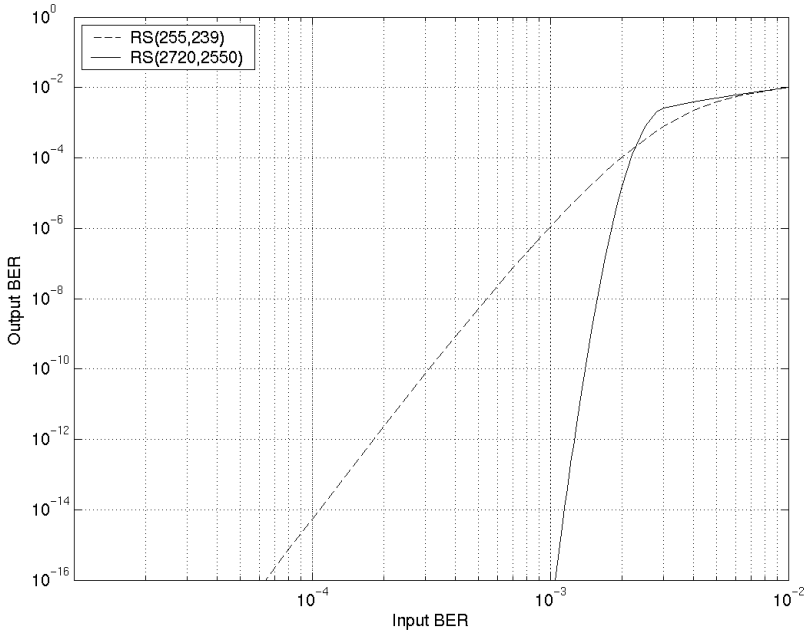

Figure I. 35/G.975.1 - Output BER as a function of the input BER for the RS (2720,2550) code and the standard FEC code

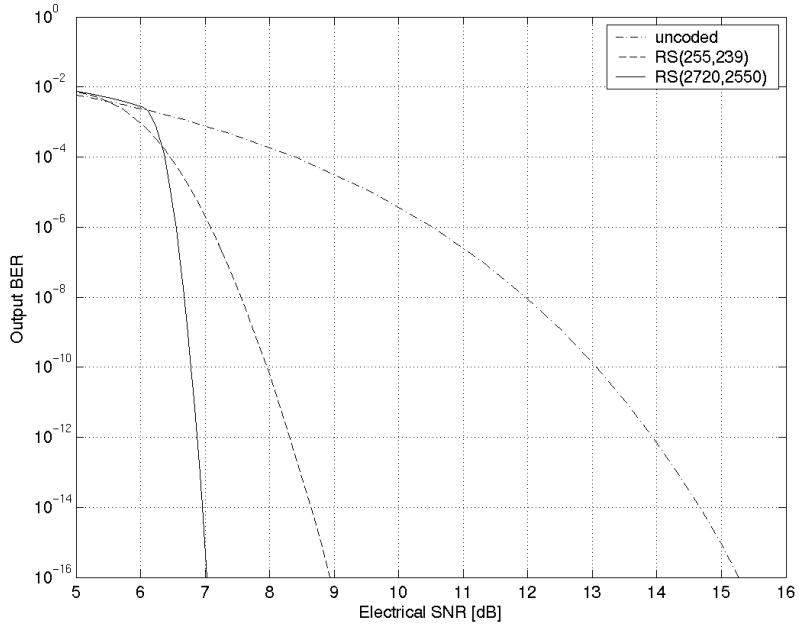

Figure I. 36/G.975.1 - Output BER as a function of the input E_b/N_0 for the RS (2720,2550) code and the standard FEC code.

Table I. 21/G.975.1 - Summary for correction ability

Input BER	Output BER	Net coding gain (dB)	Coding gain (dB)	Q limit (dB)
$1.48*10^{-3}$	10^{-9}	5.82	6.10	9.46
$1.40*10^{-3}$	10^{-10}	6.28	6.56	9.51
$1.33*10^{-3}$	10^{-11}	6.70	6.98	9.56
$1.26*10^{-3}$	10^{-12}	7.06	7.35	9.60
$1.20*10^{-3}$	10^{-13}	7.40	7.69	9.65
$1.15*10^{-3}$	10^{-14}	7.71	8.00	9.68
$1.10*10^{-3}$	10^{-15}	8.00	8.28	9.72

I.8.4 Redundancy ratio

The redundancy ratio of the Interleaved Reed Solomon (2720,2550) Code is with 7% the same as the legacy RS FEC as defined in G.975.

I.8.5 Latency

This RS (2720,2550) code with 12-bit symbols and a block length of 32640 bits and a 30592 bits is shown to have a low latency that is of the same order as for the interleaved RS (255,239) code.

I.8.6 Property

This 85-error correcting RS (2720,2550) code with 12-bit symbols has a block length of 32640 bits and a 30592 bits payload, identical to the standard RS (255,239) code. It has been shown to achieve a significant coding gain and to have superior burst correction capabilities. The encoder and decoder can be implemented efficiently in the current chip technologies for 2.5G, 10G and 40G applications, and is shown to have a low latency that is of the same order as for the interleaved RS (255,239) code.

I.9 Two interleaved extended BCH(1020, 988) super FEC code

I.9.1 Overview

The proposed FEC consists of two interleaved extended BCH(1020, 988) codes with same block-length. The Overall FEC block-length and payload length is (522240, 489472) that is in line with overhead ratio defined in G.975/G.709. The net coding gain of this code is better than 8.5 dB at BER 10-13, with a 10 times interative decoding.

I.9.2 Super FEC algorithm

The enhanced FEC scheme uses two interleaved extended BCH(1020, 988) codes with same block-length, as below described.

I.9.2.1 BCH (1020,988)

The field polynomial is:

$p(x) = x^{10} + x^3 + 1$

The code generator polynomials for the horizontal and the sloping codes are:

$g_H(x) = m_1(x)\ m_3(x)\ m_5(x)\ \ (x^2 + 1)$

$g_S\ (x) = x^{30}\ m_1\ (x^{-1})\ \ m_3(x^{-1})\ \ \ m_5(x^{-1})\ \ (x^2 + x + 1)$

being:

$m_1(x) = x^{10} + x^3 + 1$

$m_3(x) = x^{10} + x^3 + x^2 + x + 1$

$m_5(x) = x^{10} + x^8 + x^3 + x^2 + 1$

I.9.2.2 Frame structure

The payload of 16 G.709 ODUs is collected in order to build a BCH super frame. So there are 3824 bit vectors containing 128 bits each, indexed according to the order of transmission, forming the following 512×956 bit-matrix.

0	4	8				24		3800				3816	3820
1	5	9				25		3801				3817	3821
2	6	10				26		3802				3818	3822
3	7	11				27		3803				3819	3823

The overall frame (512×1020 matrix) is obtained by appending 512×64 parity bits, i.e. by adding 64 columns at the right side.

The order of transmission of the data bits is preserved.

I.9.2.3 Interleaving function

The overall frame, composed of 512×1020 bits, is divided into 16×32 sub-blocks. The rows are padded with four bits set to zero, adding four columns at the left side of the structure; obviously, those bits aren't transmitted.

Each sub-block is a square containing 32×32 bits.

The blocks on the columns 2,3...31 contain the payload bits, while the blocks on the columns 0-1 contain the parity bits.

0,31	0,30	0,29	0,28	0,27
1,31	1,30	1,29	1,28	1,27
2,31				
14,31	14,30	14,29	14,28	14,27
15,31	15,30	15,29	15,28	15,27

0,4	0,3	0,2	0,1	0,0
				14,0
15,4	15,3	15,2	15,1	15,0

The interleaving function shifts the blocks inside each column, giving the following matrix,

15,31	15,30	14,29	14,28	13,27
0,31	0,30	15,29	15,28	14,27
1,31	1,30	0,29	0,28	15,27
2,31	2,30	1,29	1,28	0,27
				1,27
				2,27
				3,27
				4,27
				5,27
8,31	8,30	7,29	7,28	6,27
				7,27
				8,27
				9,27
				10,27
13,31	13,30	12,29	12,28	11,27
14,31	14,30	13,29	13,28	12,27

2,4	1,3	1,2	0,1	0,0
3,4	2,3	2,2	1,1	1,0
4,4	3,3	3,2	2,1	2,0
5,4				
6,4				
7,4				
8,4				
9,4				
10,4				
11,4	10,2	10,2	9,1	9,0
12,4				
13,4				
14,4	13,3	13,2	12,1	12,0
15,4	14,3	14,2	13,1	13,0
0,4	15,3	15,2	14,1	14,0
1,4	0,3	0,2	15,1	15,0

Also, the interleaving function shifts the bits inside the columns of each block. So the following block

0,31	0,30	0,29	0,2	0,1	0,0
1,31	1,30	1,29			1,0
2,31	2,30	2,29			2,0
					29,0
					30,0
31,31	31,30	31,29	31,2	31,1	31,0

Becomes:

0,31	31,30	30,29	3,2	2,1	1,0
1,31	0,30	31,29	4,2	3,1	2,0
2,31	1,30	0,29	5,2	4,1	3,0
29,31	28,30	27,29	0,2	31,1	30,0
30,31	29,30	28,29	1,2	0,1	31,0
31,31	30,30	29,29	2,2	1,1	0,0

The interleaving function can be also expressed with a simple formula; the bit lying in the position [I,J], (with $0 \leq I \leq 511$, $0 \leq J \leq 1023$) goes in the position:

[((I-J-1 MOD 32) + 32 (I/32 - J/64) MOD 512), J], with "/" representing integer division.

The parity bits are computed with the constraint that, every row (there are 512 rows) of the overall frame is a BCH(1020,998) codeword and, every row (there are 512 rows) of the interleaved overall frame is a BCH(1020,998) codeword. It follows that every transmitted bit is protected by two BCH codes.

A key property of this interleaving function is that the column index remains unchanged. This allows the horizontal and sloping BCH encoders to process in parallel the same incoming data bits, without intermediate storage.

Columns from 0 to 63 contain the parity bits, and are transmitted interleaved with data in order to preserve the standard data structure, that is each ODU is followed by 2048 bits belonging to the same overall frame.

The order of transmission order of the parity bits is as follows

For T=0 to 32767

Row = T MOD 64 + 64 (T / 4096)

Column = 63 - (T MOD 4096) / 64

Send_bit(Row, Column)

End

I.9.2.4 Encoder

The final result of this process is to obtain that each row is a BCH codeword both before and after the interleaving function. We obtain that using superposition of effects.

Consider the parity blocks (0,1) and (0,0), the same process is repeated on the remaining 15 block rows.

First consider the horizontal code; block (0,1) is set to zero (1024 zeros) and for each of the 32 rows the remainders by $g_H(x)$ are carried out. This 1024 bits result is collected in the vector p_H.

The sloping code works on the rows the interleaved frame; note that the parity blocks have the same position. Block (0,1) is set to zero, and for each of the 32 rows the remainders by $g_S(x)$ are carried out. This 1024 bits result is collected in the vector p_S.

Now, the bits inside the block (0,1), denoted as vector q, are constrained to give the same total parity for both codes.

Named M_H and M_T as the linear operators representing the remainder operation from block (0,1) to block (0,0), and T as the interleaving matrix, we have:

$$T\,(M_H\,q + p_H) = M_S\,T\,q + p_S \quad \Rightarrow \quad q = (T\,M_H - M_S\,T)^{-1}\,(p_S - T\,p_H)$$

Finally, the content of the blocks (0,1) and (0,0) are set to be, respectively, q and $M_H\,q + p_H$.

I.9.2.5 Iterative decoding

Clearly, error correction capability increases with the number of iterations. This number can be vendor specific. However, due to the simplicity of the interleaving function and the low degree of the BCH polynomials, a number of 12 to 20 iterations can be easily reached.

Decoding by erasure filling is also possible and suggested. For example the most probable error pattern that is not correctable by the BCH decoders, is composed by 8 bit error belonging to a couple of horizontal code-words and a couple of sloping code-words; this pattern is easily recognized and corrected. Similar, and minor order error patterns can be filled with a low complexity erasure algorithm.

I.9.3 Error correction ability

Error correction capabilities of this enhanced FEC scheme depends on the number of iteration used in the decoding process. When a 10 times iterative decoding process is implemented , the performances of the code are listed in Table I. 22 (Results are derived from simulations).

Table I. 22/G.975.1 - Summary for correction ability

Input BER	Output BER	Net coding Gain (dB)	Coding Gain (dB)	Q factor (dB)
5.00E-03	3.07E-03	0.25	0.54	8.22
4.70E-0.3	8.87E-04	1.33	1.61	8.29
4.50E-03	4.42E-05	3.25	3.53	8.34
4.30E-03	9.30E-08	5.67	5.95	8.39
4.00E-03	7.00E-14	8.63	8.91	8.47
3.50E-03	2.10E-14	8.67	8.95	8.62

In case an erasure algorithm is used, as previously suggested, performance can be impoved, obtaining, e.g., an output BER less than 10E-16 for an input BER equal to 4.00E-03.

Figures I. 37 and I. 38 represent the performances of the described enhanced FEC, in terms of BER versus Q factor and in terms of Output BER versus Input BER.

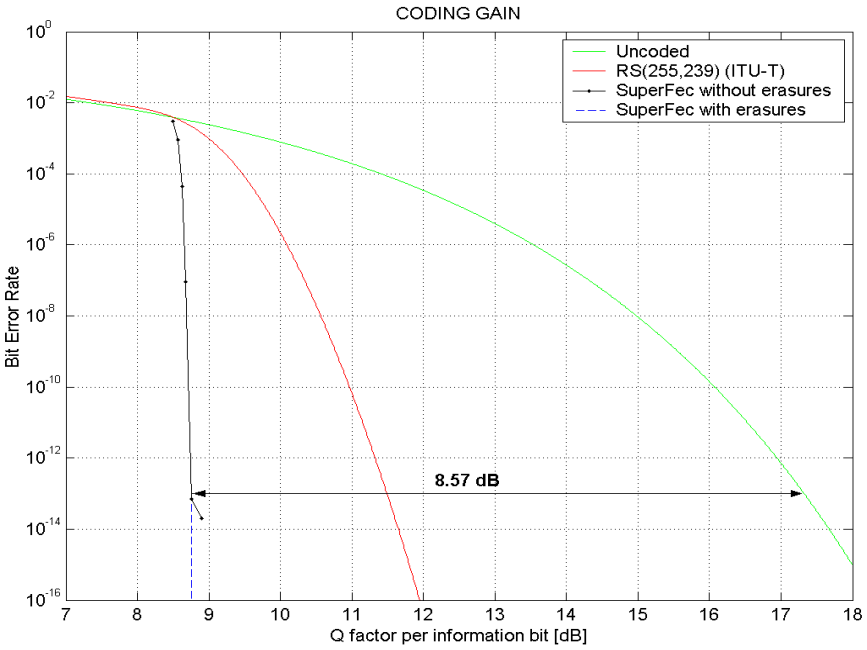

Figure I. 37/G.975.1 – Coding Gain

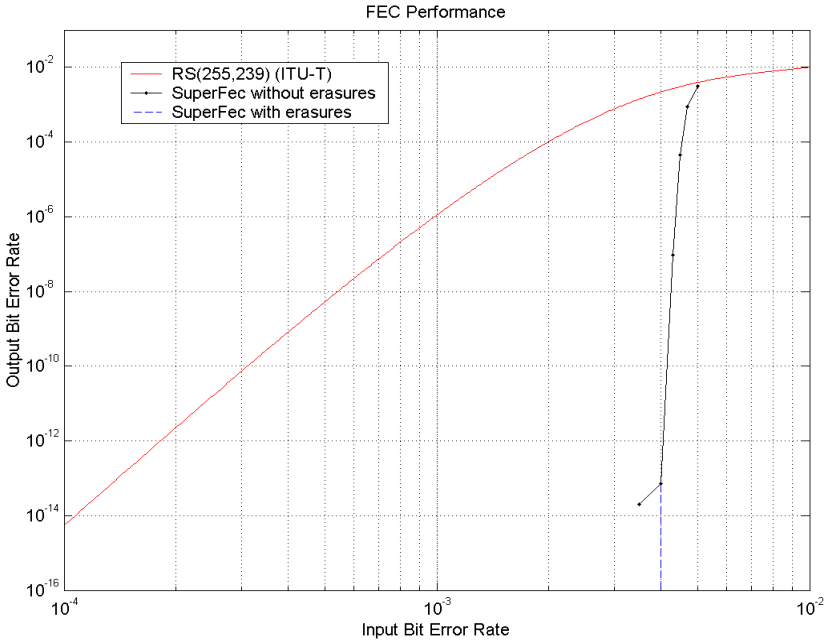

Figure I. 38/G.975.1 – FEC Performance

I.9.4 Redundancy ratio

The redundancy ratio of the described coding scheme is equal to 6.69%, equal to the standard RS(255,239) described in recommendation G.709.

I.9.5 Latency

The latency for a 10Gbit/s payload is around 50µs for the encoder, while for the decoder is around 100 µs.

I.9.6 Property

The enhanced FEC scheme generates a coded signal bit rate is exactly the bit rate defined by G.709. Moreover, despite the great block-length, the decoding machine can be implemented with a very low number of circuit elements.